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M2A.5

Low-Voltage, Complex-DSP-Free 200G PAM4 / 140G OOK Operation of Si Photonic Crystal Slow-Light Modulator with Built-in EO Equalizer

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[4] Photonics Electronics Technology Research Association (PETRA)

Optical Fiber Communication Conference (OFC) 2026

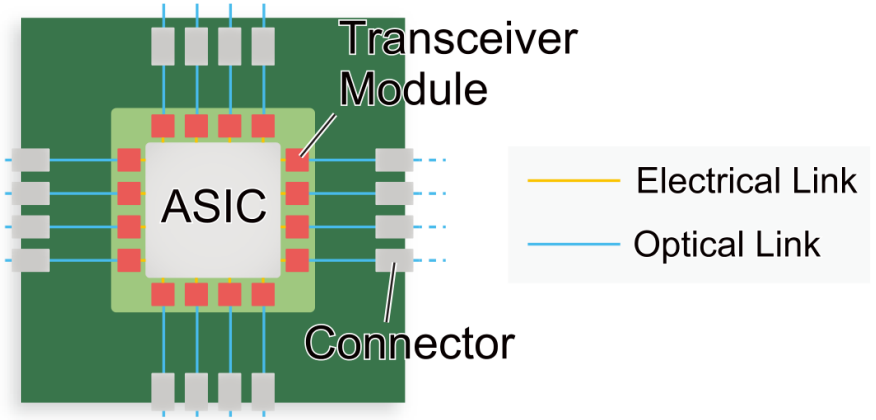
Mar. 16, 2026

Los Angeles Convention Center | Los Angeles, California, United States

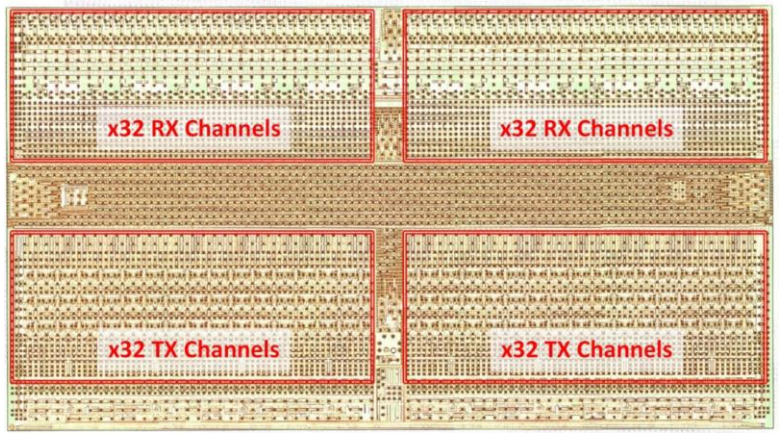
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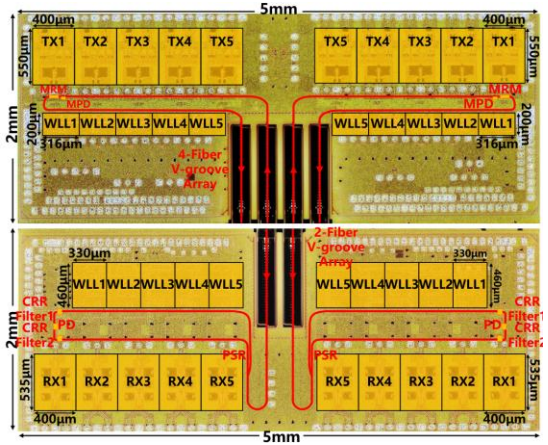
Co-Packaged Optics (CPO)



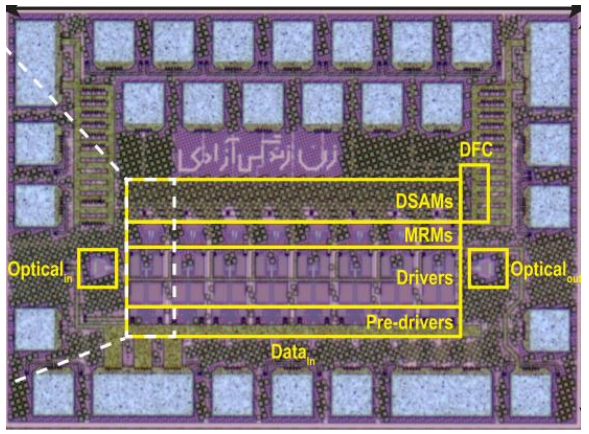
High speed, Low power, and Small footprint ➡ Silicon Photonics Transceivers



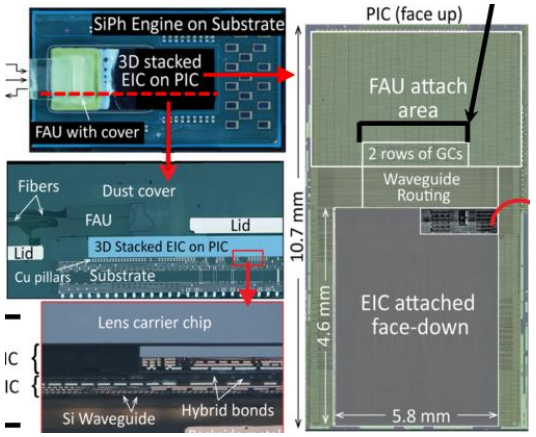
[ISSCC'26 Broadcom**]**



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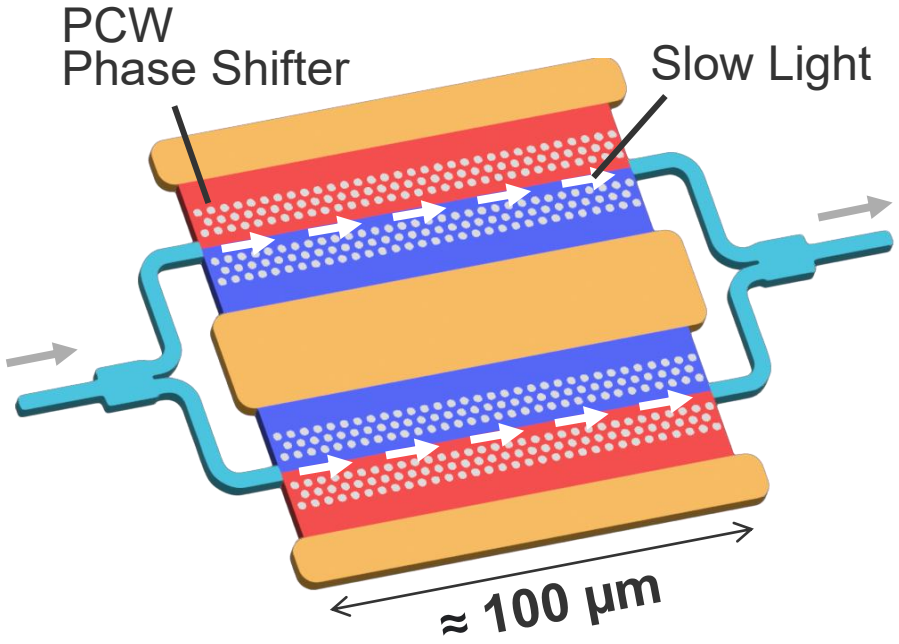
[ISSCC'26 UPenn**]**



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Si Photonic Crystal Waveguide（PCW）MZM

Slow light enhances modulation efficiency

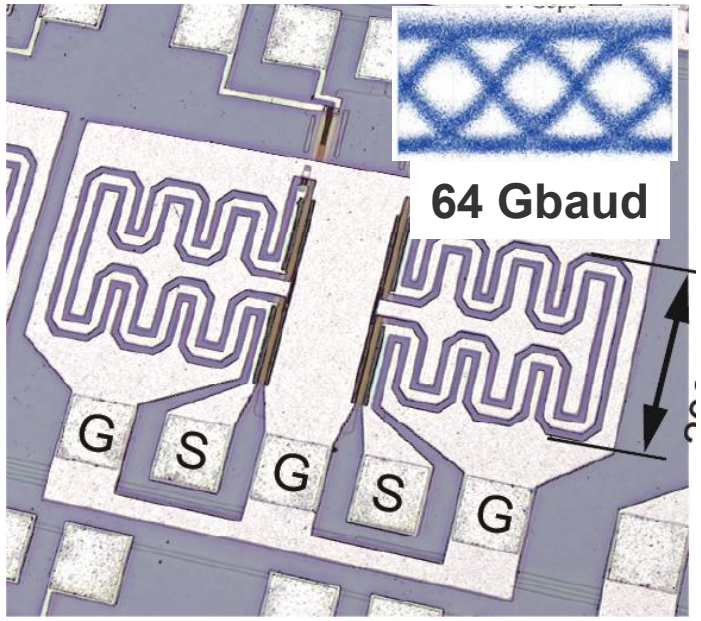


[H. C. Nguyen, *et al.*, *Opt. Express*, vol. 19, no. 14, p. 13000, Jul. 2011.]

😊 **Small Footprint**

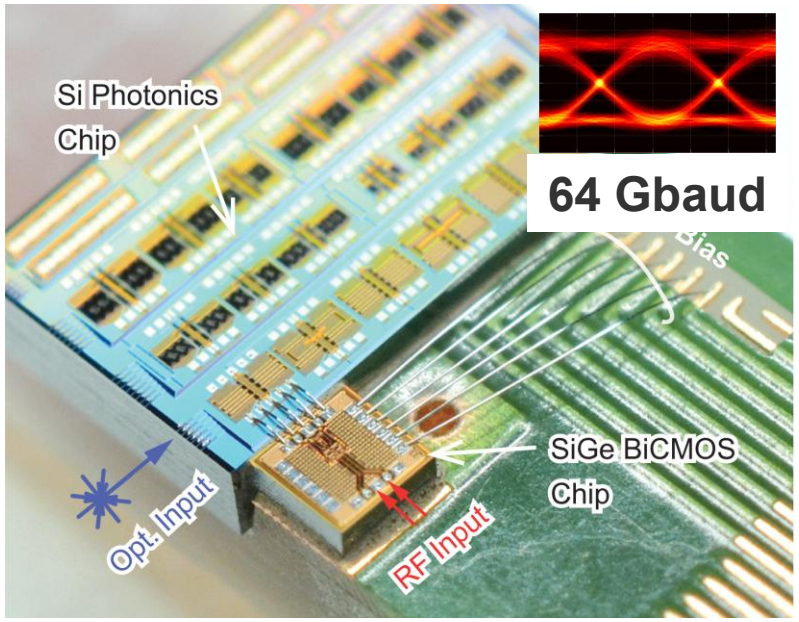
😊 **Moderate Operating λ Range**

Bandwidth extension by EO phase matching



[Y. Hinakura *et al.*, *IEEE JSTQE*, vol. 27, no. 3, May 2021.]

High-efficiency modulation with a co-designed driver



[K. Kawahara *et al.*, *IEEE JSTQE*, vol. 32, no. 2, Jan. 2026.]

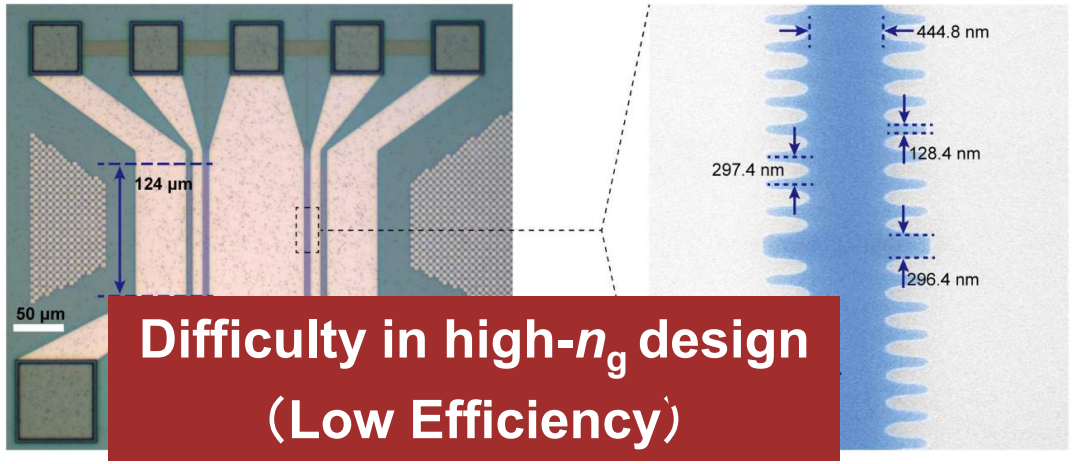
Previous results are limited to **64 GBd**

BW is limited by the $R_{pn}C_{pn}$ **time constant**

Challenges in High-Speed Slow-Light Modulators

Slow-light MZMs using Bragg CROW → Small RC constant due to strong optical confinement

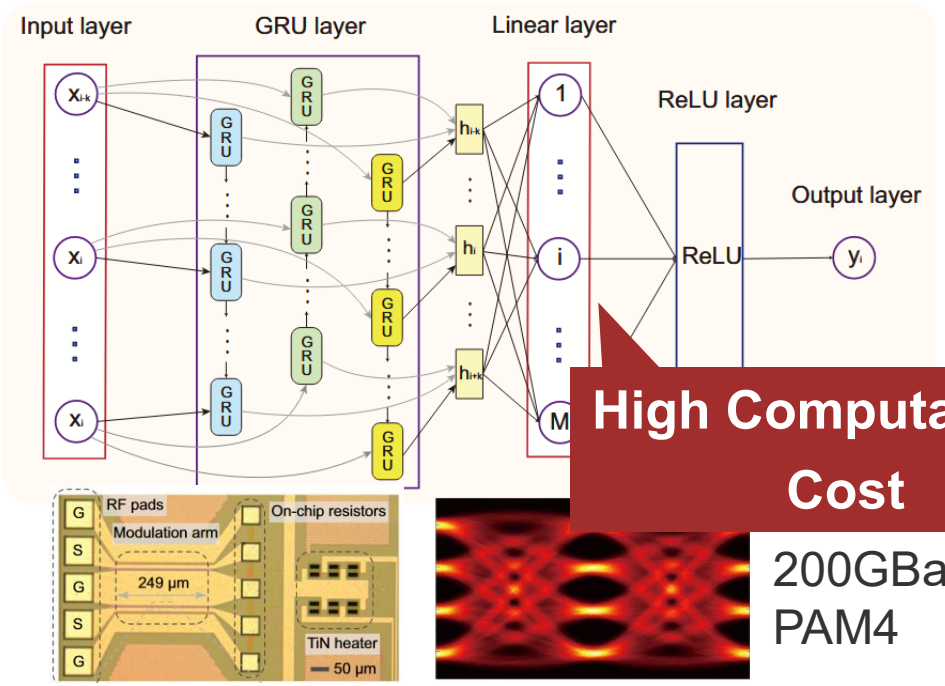
Peking Univ. ’23: 112GBaud NRZ（V_{pp} = 5 V）



Difficulty in high-n_g design（Low Efficiency）

C. Han *et al.*, *Science Advances*, vol. 9, no. 42, Oct. 2023.

Peking Univ. ’25: 200GBaud PAM4（w/ **NN-DSP**）



High Computational Cost

200GBaud PAM4

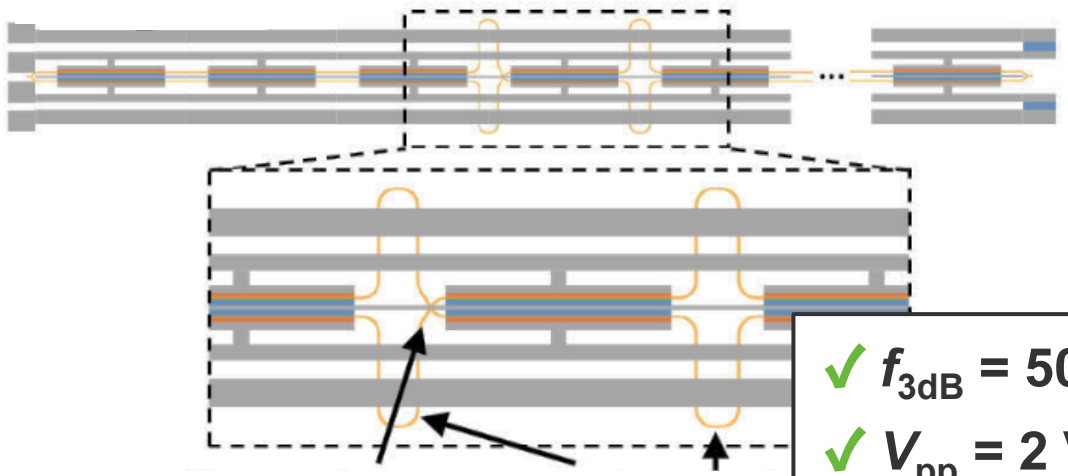
C. Han *et al.*, *Nature Communications*, vol. 16, no. 1, Jul. 2025.

😢 **Reliance on high drive voltage (V_{pp} = 5 V) and power-hungry DSP**

Bandwidth Extension via EO Equalizer

Optical and electrical delays form an FIR filter → 😊 Eliminate DSP reliance

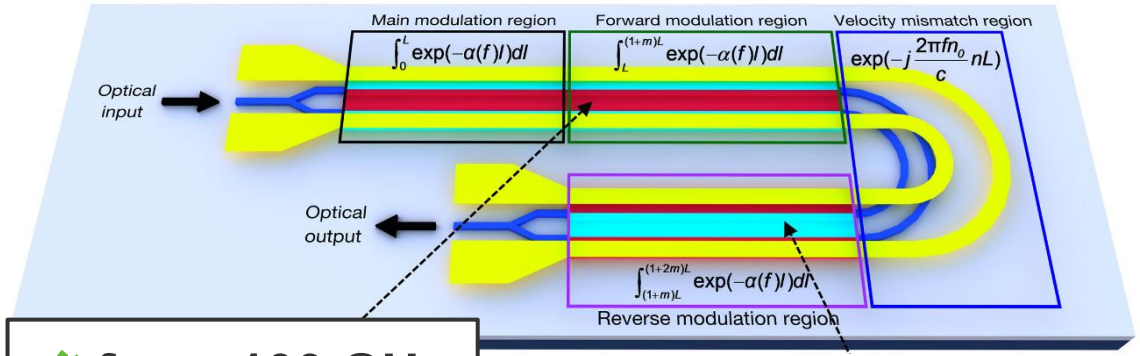
Using **Optical Crossing**: Ghent Univ. ’21



✓ f_{3dB} = 50 GHz
✓ V_{pp} = 2 V
😢 L = 2.5 mm

L. Breyne *et al.*, *J. Light. Technol.*, vol. 39, no. 6, Mar. 2021.

Using **Reverse Doping**: ZJU ’25



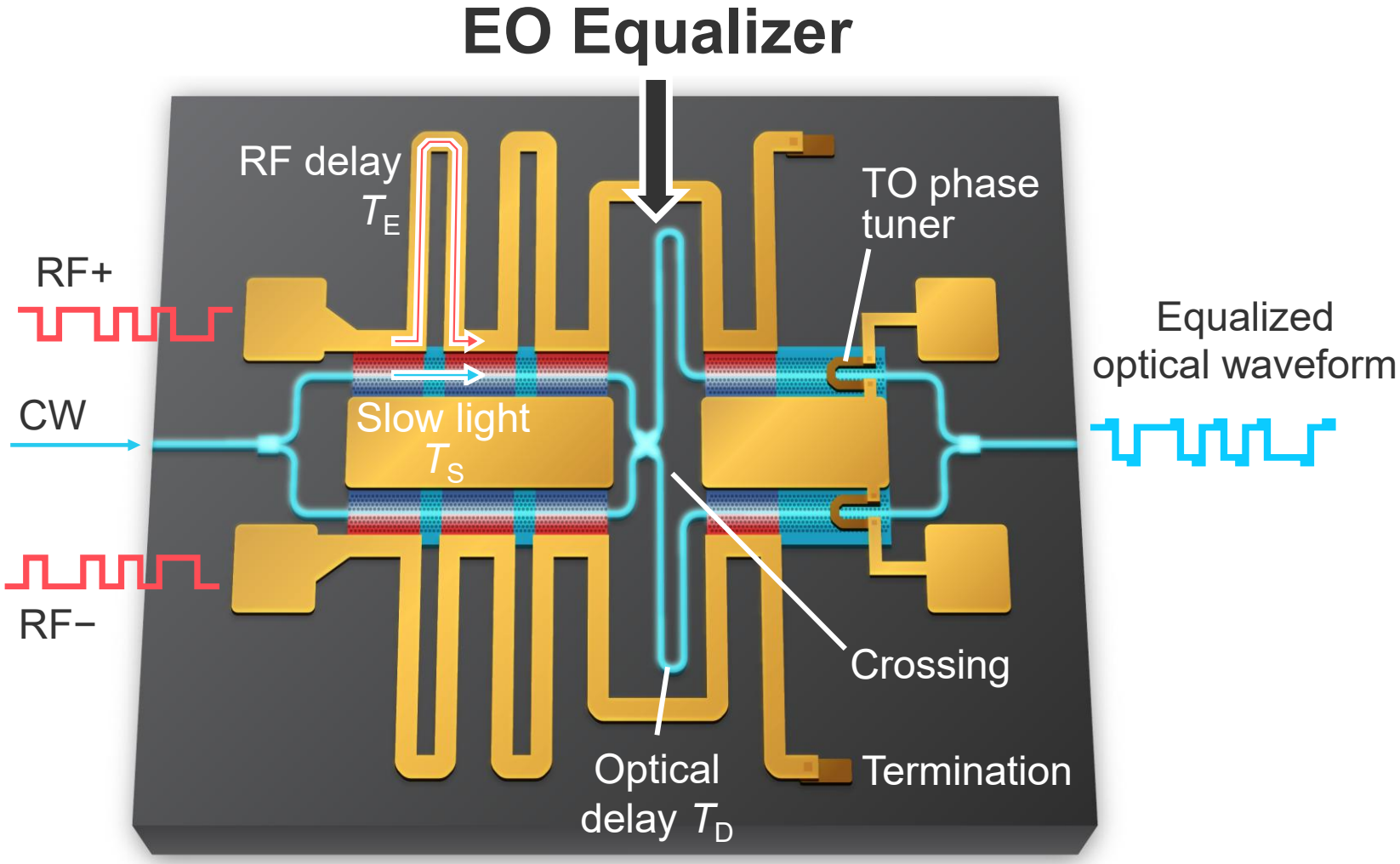
✓✓ f_{3dB} > 100 GHz
😢 V_{pp} = 5 V
😢 L = 2.5 mm

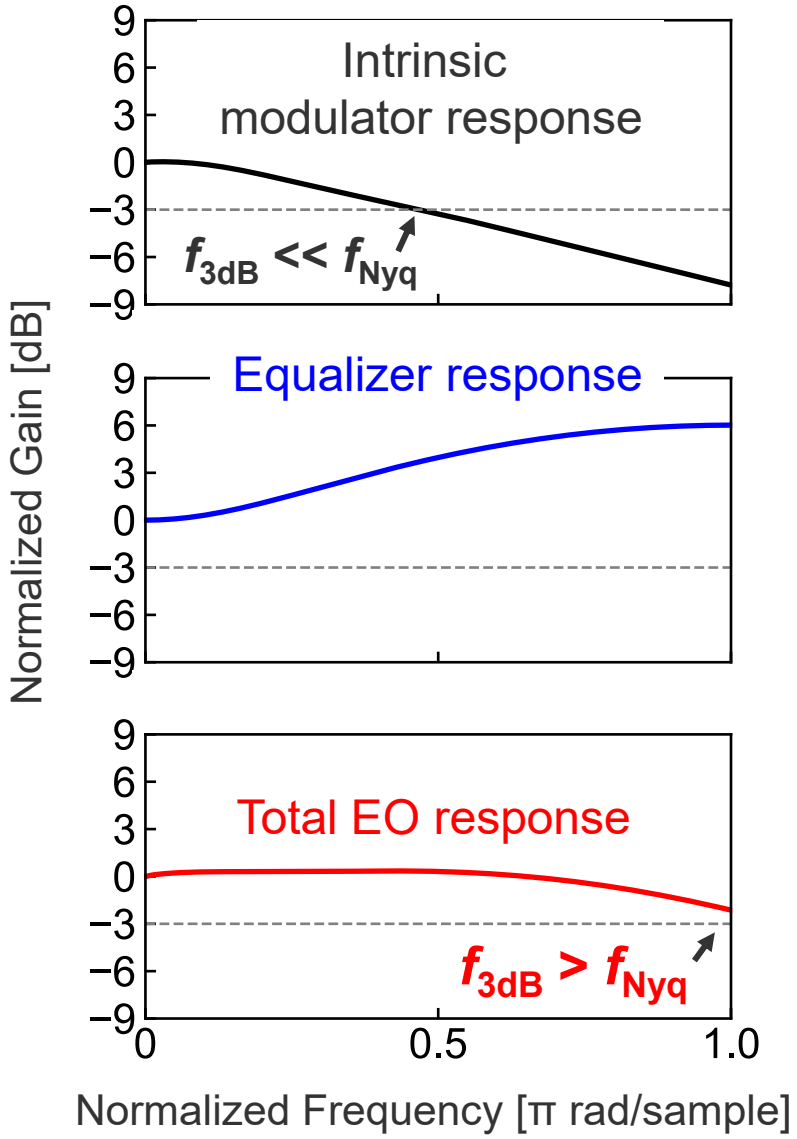
H. Yue *et al.*, *Optica*, vol. 12, no. 2, Feb. 2025.

😢 **Long phase shifters are required to maintain V_π → Large footprint**

(Typically, ***L* > 2 mm** for rib-type phase shifters)

Proposed Si PCW MZM with EO Equalizer



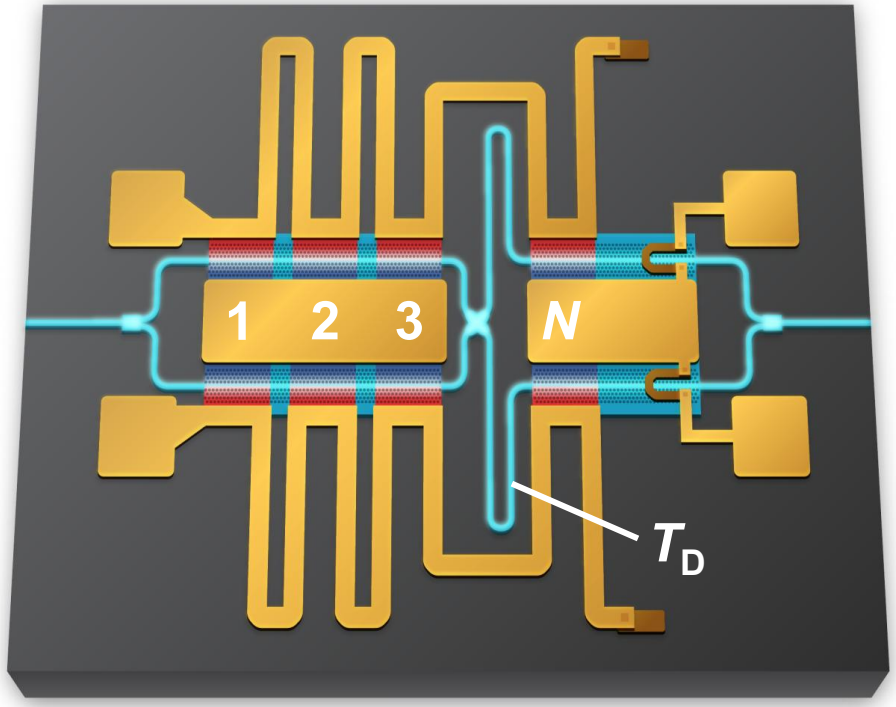


➡ Enables **200G/λ** operation **independent of DSPs**

Design of the EO Equalizer

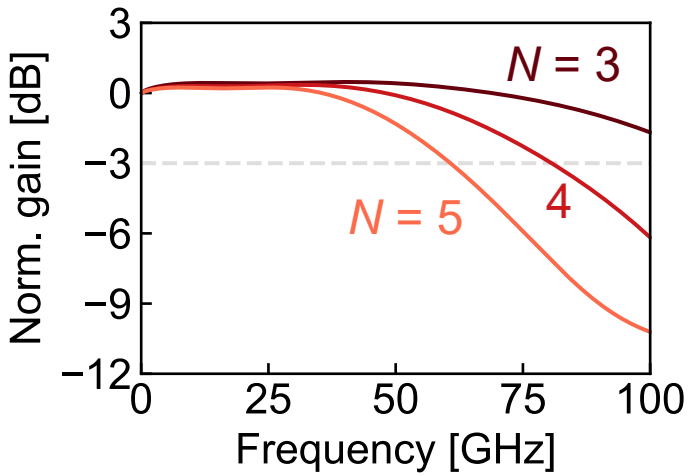
Design parameters

① ***N*** segments ② Tap delay T_D

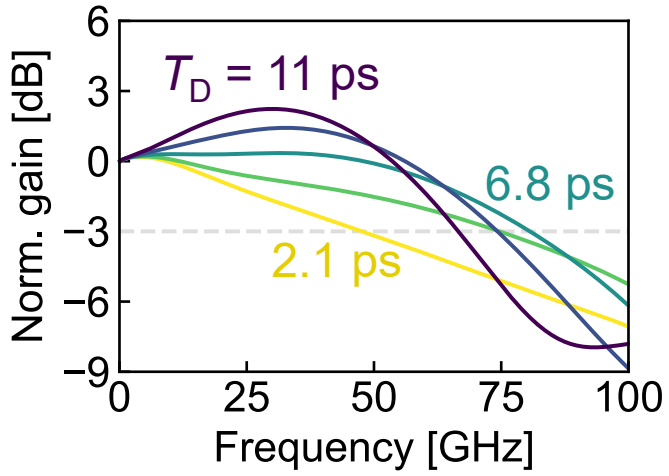


$$\frac{H(\omega)}{\Delta\varphi} = (\boldsymbol{N} - 1) - e^{j\omega \boldsymbol{T_D}}$$

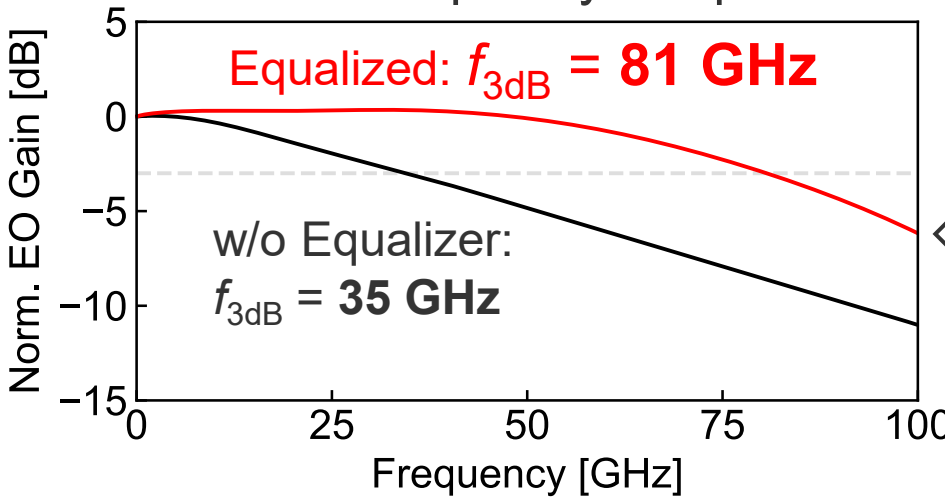
Peak gain tuning via ***N***



Peak freq. tuning via T_D



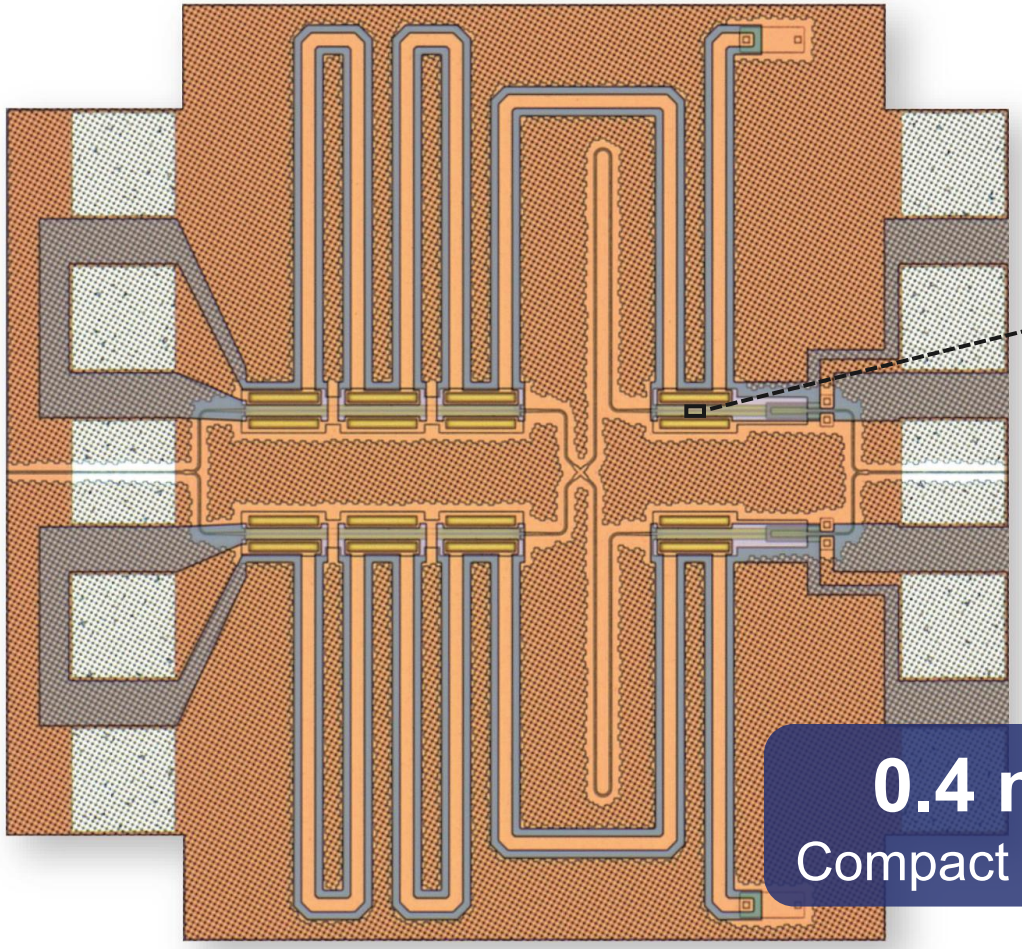
Overall frequency Response



N = 4
T_D = 6.8 ps

Fabricated Si PCW Modulator

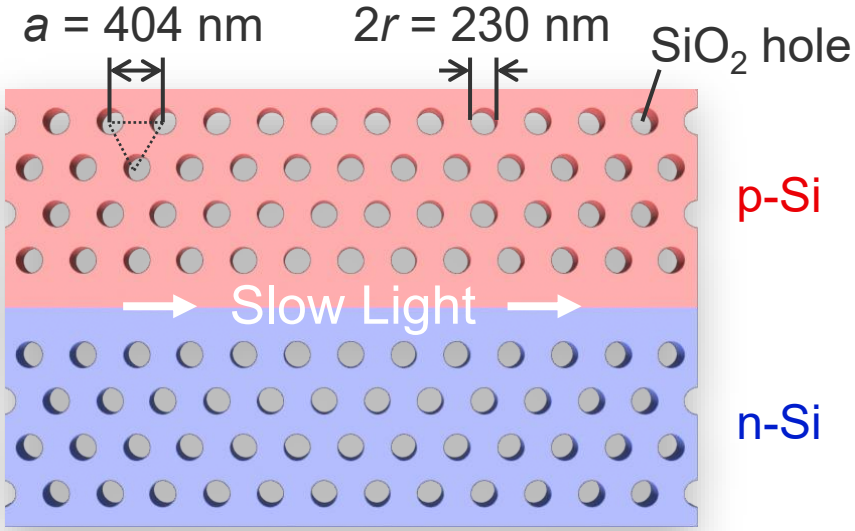
300-mm SOI-Wafer Si Photonics Process

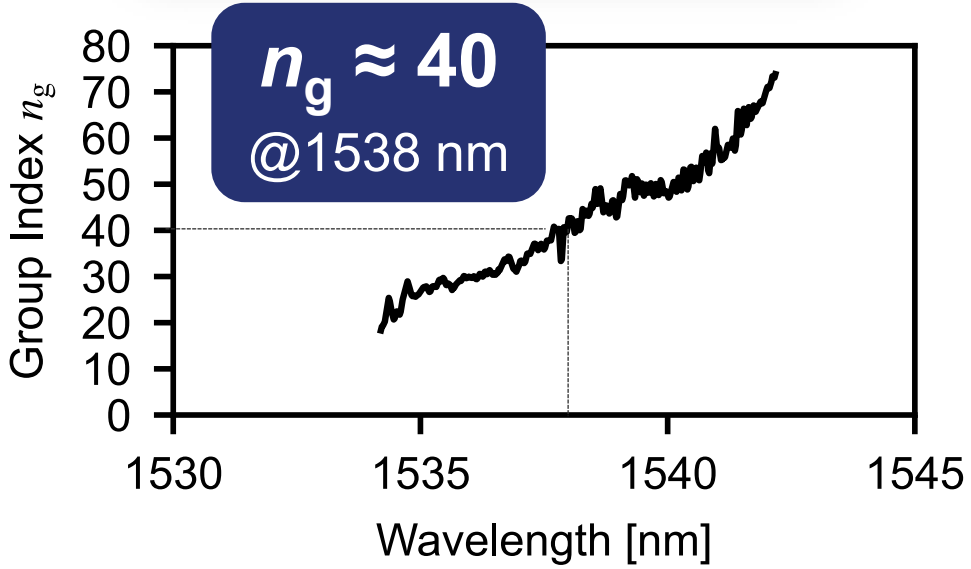


p-n-doped PCW phase shifter

Output

0.4 mm²
Compact Footprint

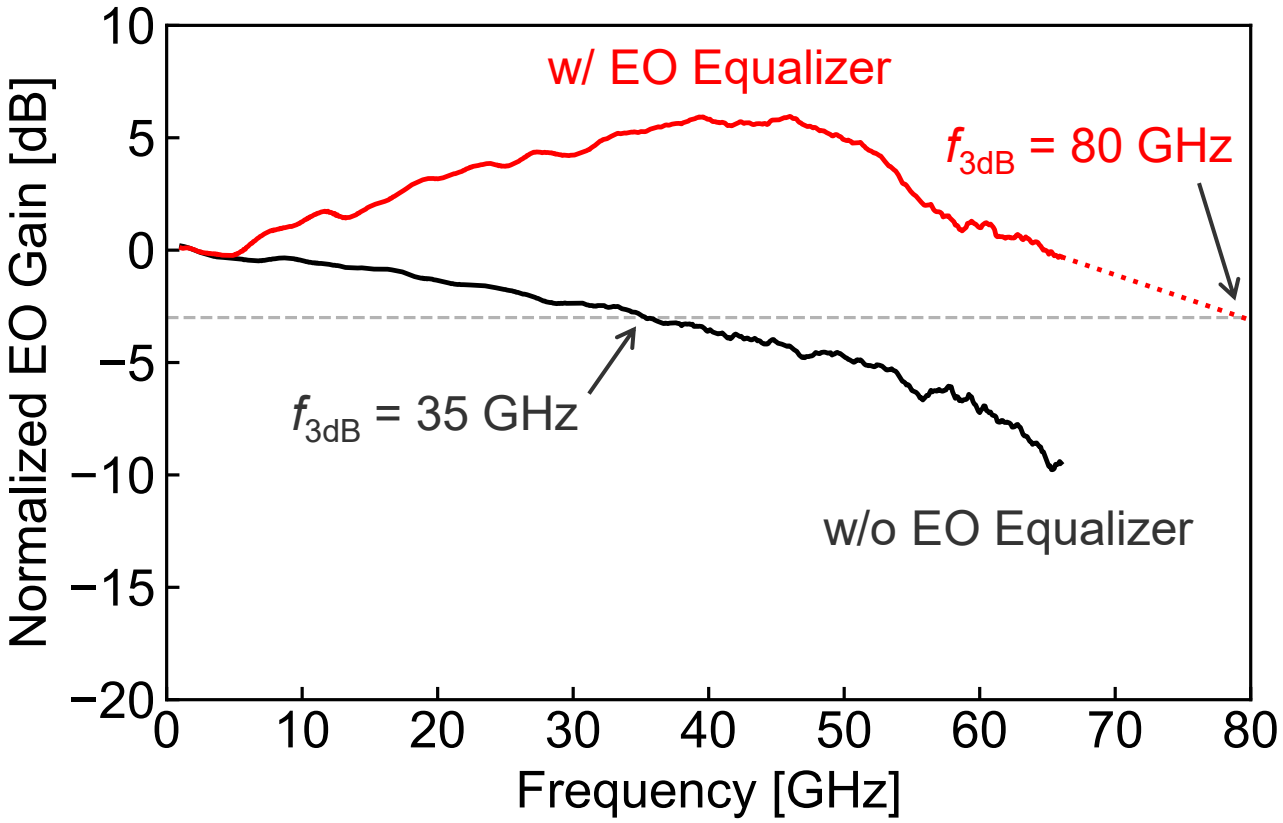




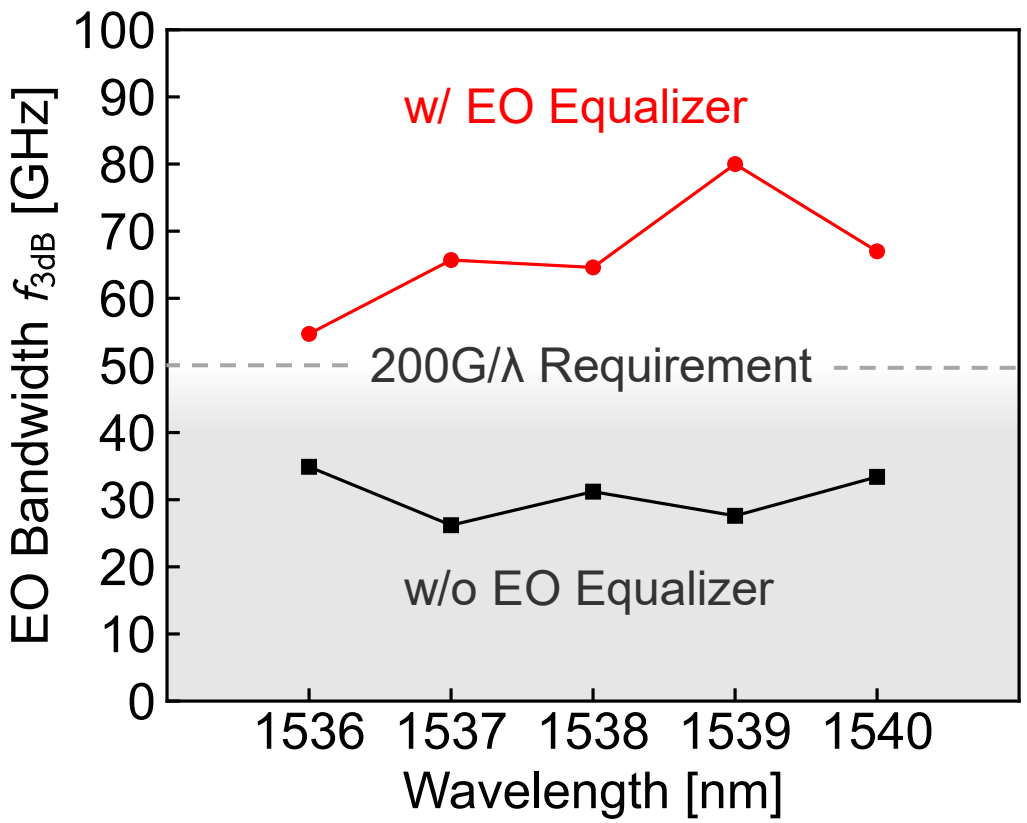
EO Frequency Response

Measured by Keysight N5227B & N4373E (***N*** **= 3,** L_{Total} **= 150 μm,** R_T **= 50 Ω,** V_{DC} **= −3.5 V**)

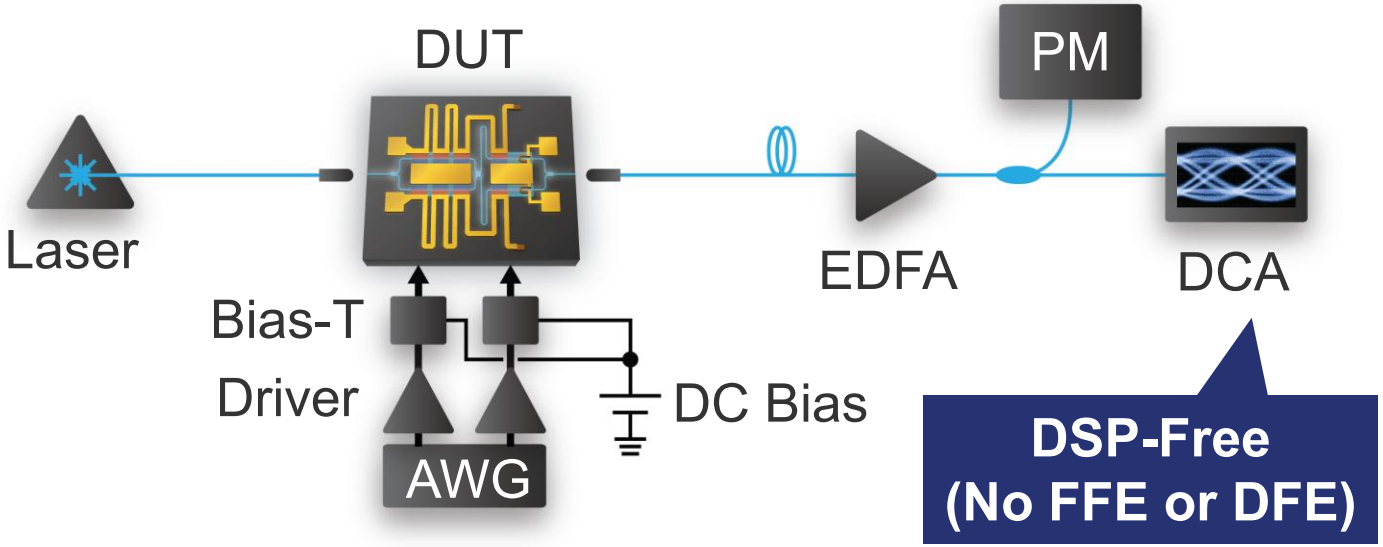
EO equalizer extended the BW **from 35GHz to 80GHz**



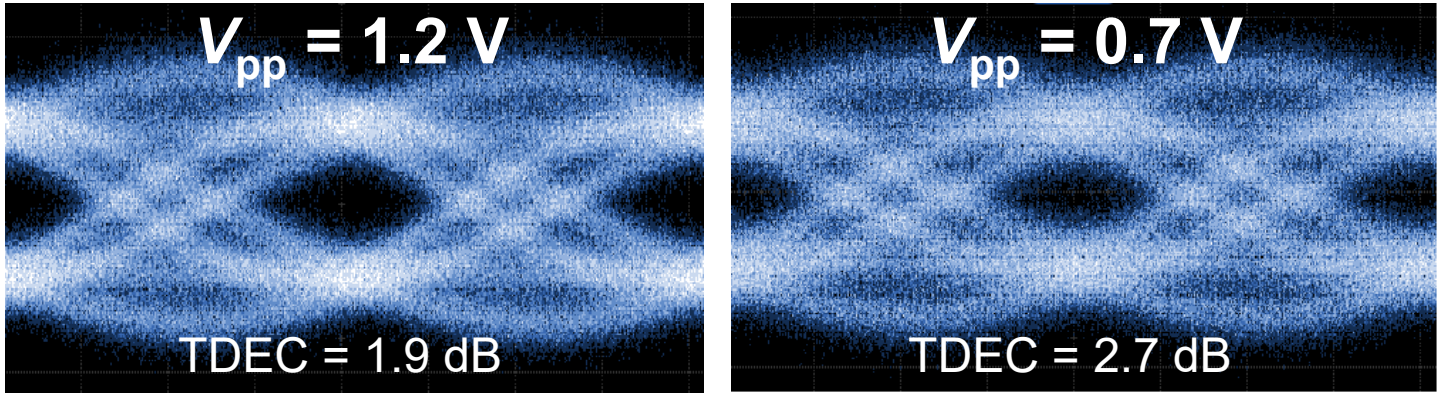
Satisfy 200G/λ requirement for overall operating wavelength of the PCWs



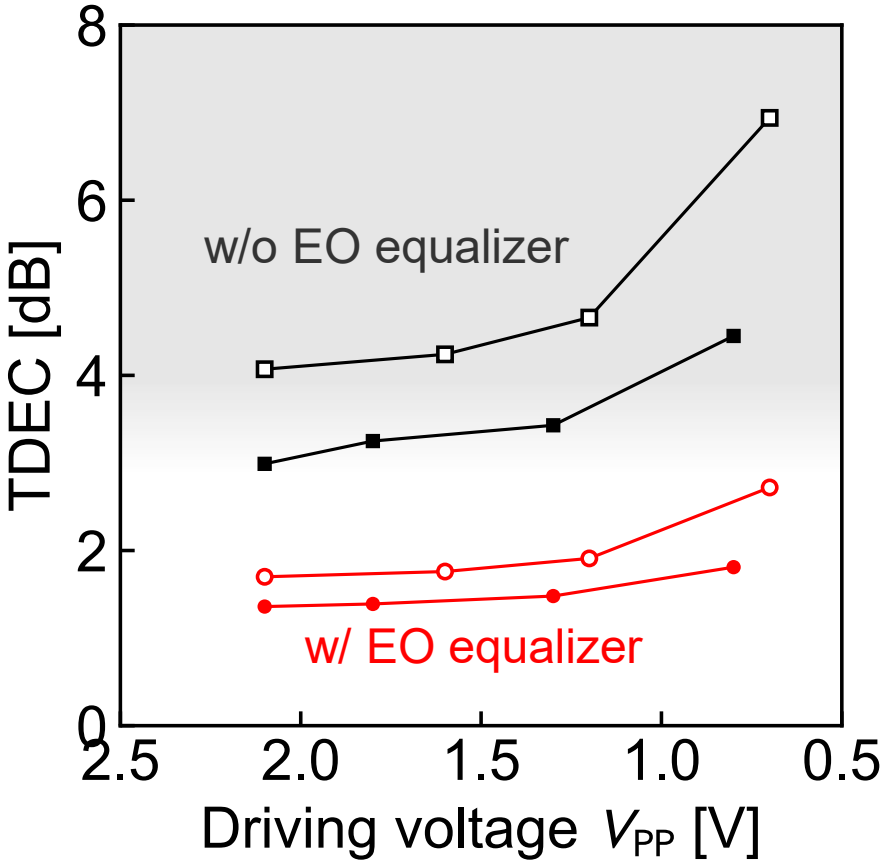
DSP-Free OOK Eye Diagram



112-Gb/s OOK

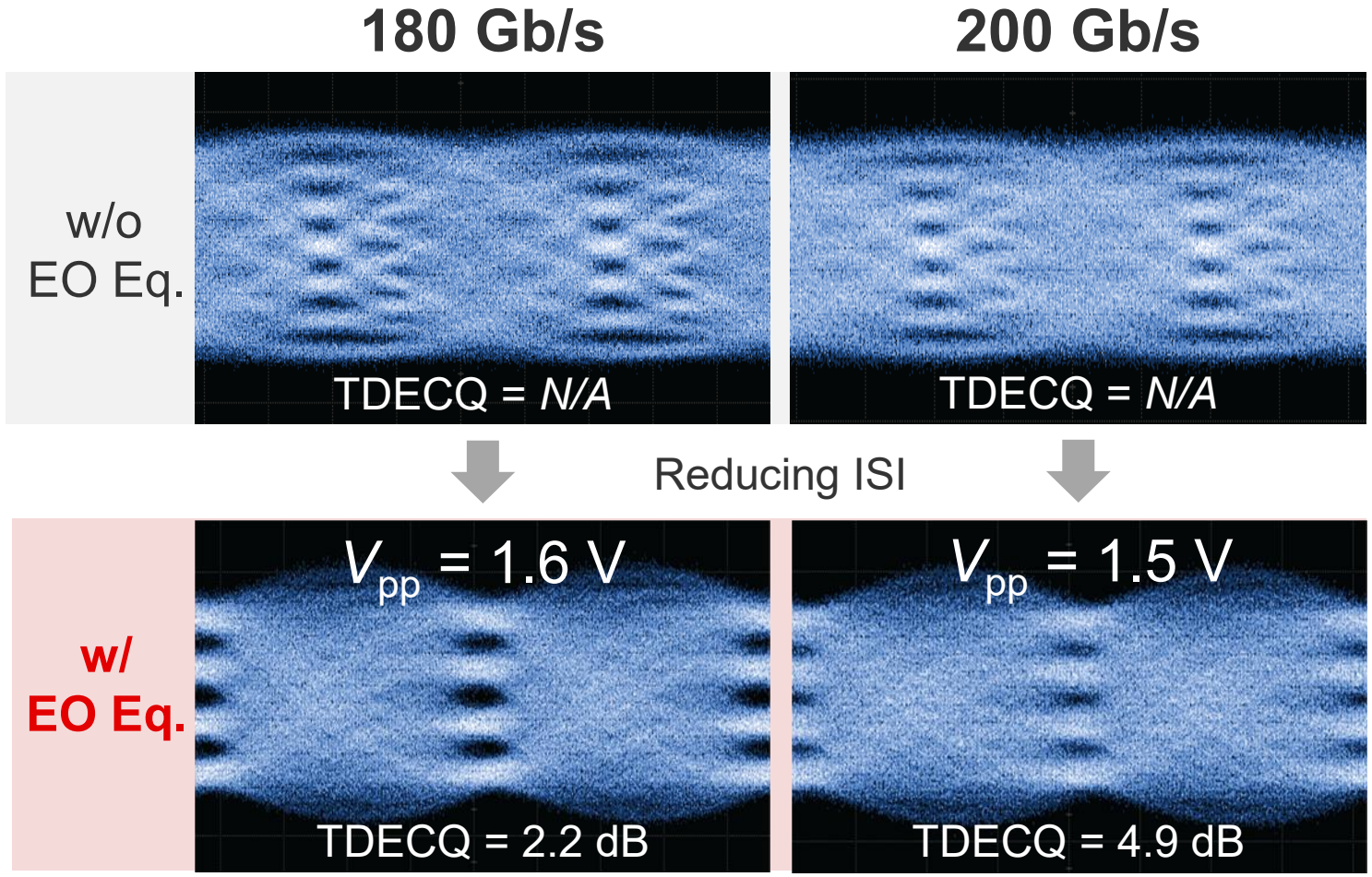


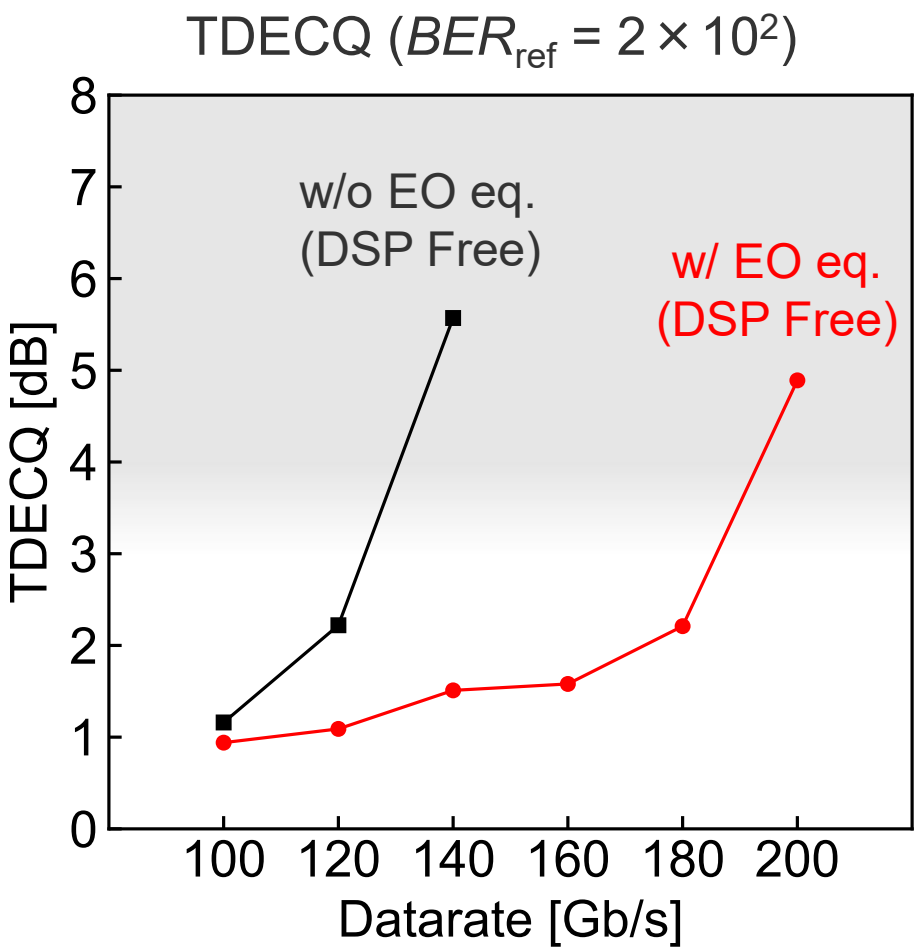
TDEC ($BER_{ref} = 2 \times 10^{2}$) at **112 Gb/s**



EO equalizer improves TDEC and enables direct driving by CMOS

DSP-Free PAM4 Eye Diagram



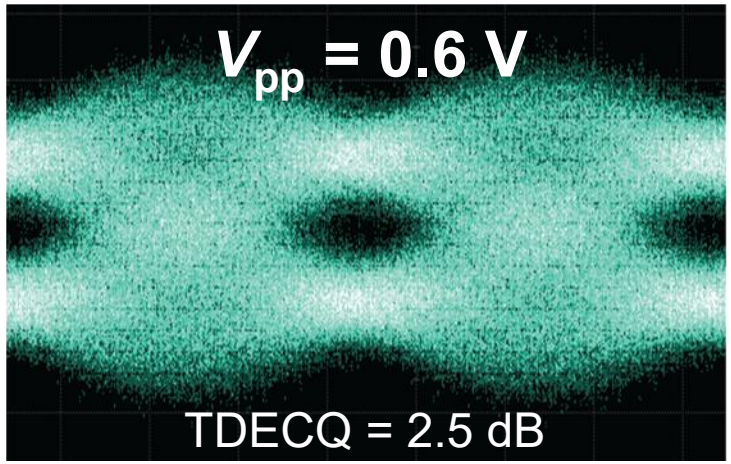


Inter-symbol interference is suppressed, and clear eye opening is observed at up to 180 Gb/s

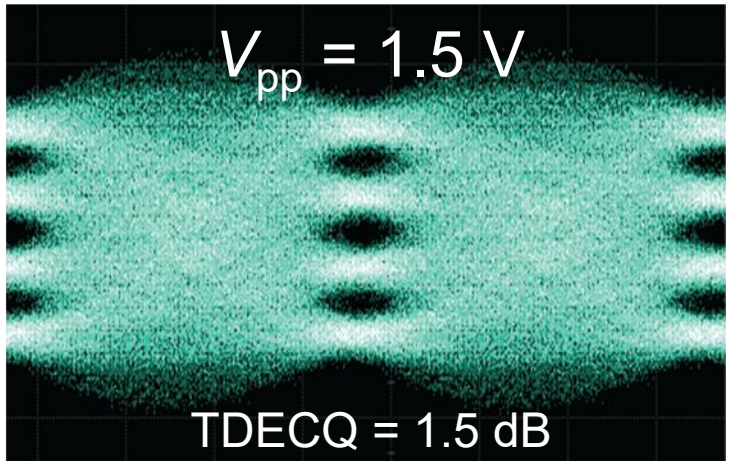
Eye Diagram with Light DSP

Applied only a practical **11-tap FFE** at receiver

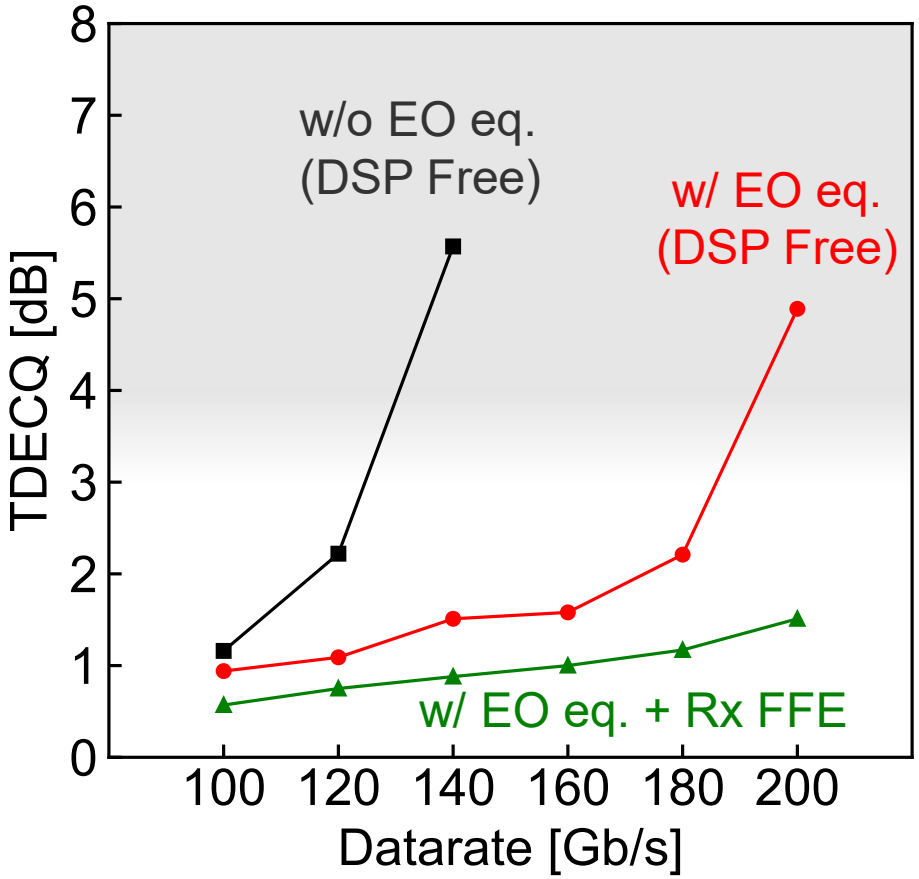
140 Gb/s OOK



200 Gb/s PAM4



PAM4 TDECQ ($BER_{ref} = 2 \times 10^{2}$)



Data rate extended to **140 Gb/s for OOK** and **200 Gb/s for PAM4** with light DSP

Conclusion

Si Photonic Crystal Slow-Light MZM with Built-in EO Equalizer

- ✓ EO equalizer extended the BW **from 35GHz to 80GHz**
- ✓ **DSP-free 112-Gb/s OOK** (V_{pp} ≈ 0.7 V) and **180-Gb/s PAM4**
- ✓ **200-Gb/s PAM4** with DSP-light

→ Promising candidate for energy-efficient multi-Tb/s interconnects

Acknowledgement

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- The authors would like to thank Keysight for lending the arbitrary waveform generator and digital communication analyzer used in this experiment, and Lumentum Japan Inc. for their financial support.