Optical Transmitter with Silicon Slow-Light Modulator and BiCMOS Current-Mode Driver Achieving 0.78 pJ/bit Total Bit Energy and 0.66 mm^2 Footprint

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OECC / PSC 2025

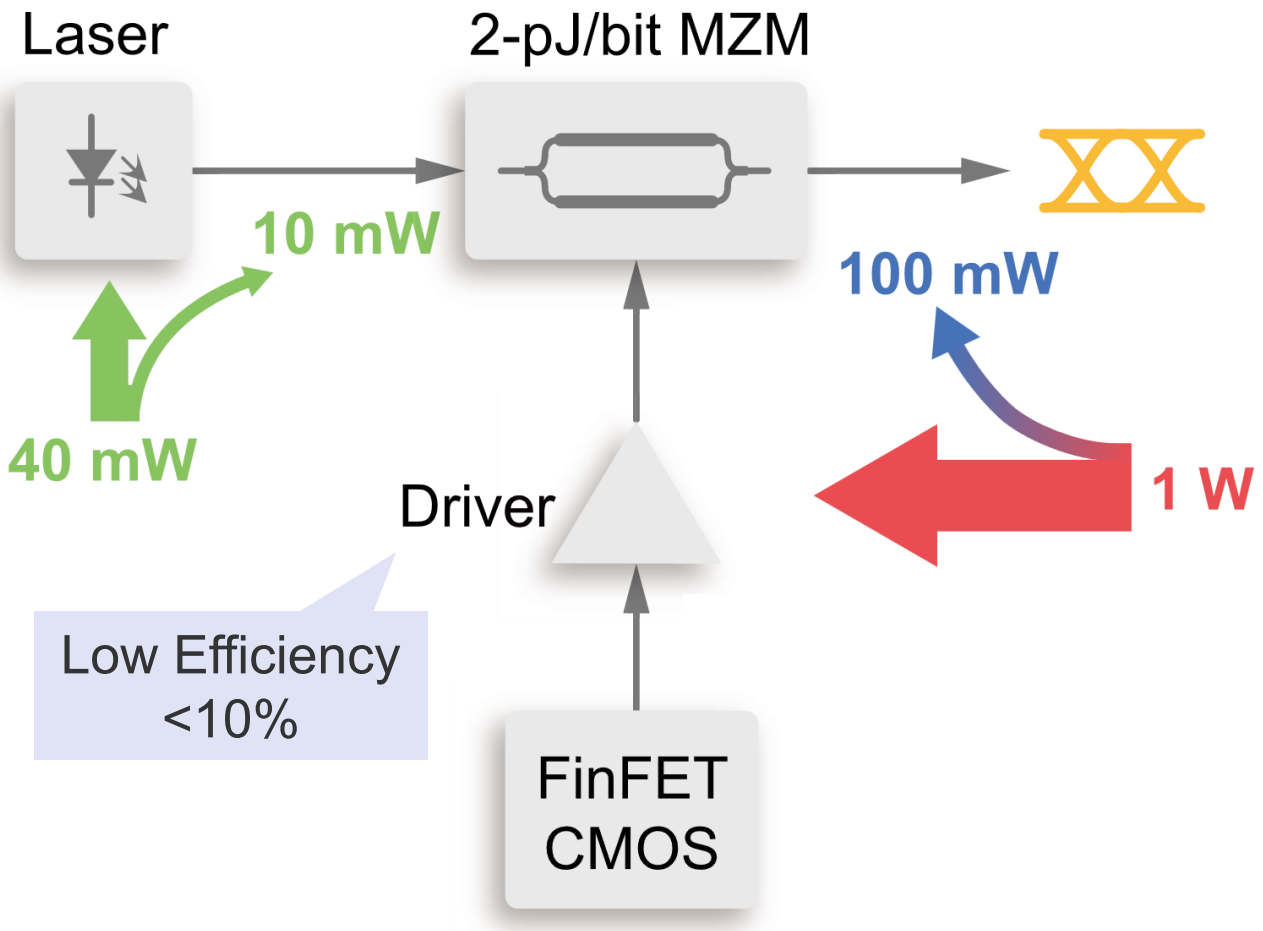
2025/7/3, Sapporo Convention Center

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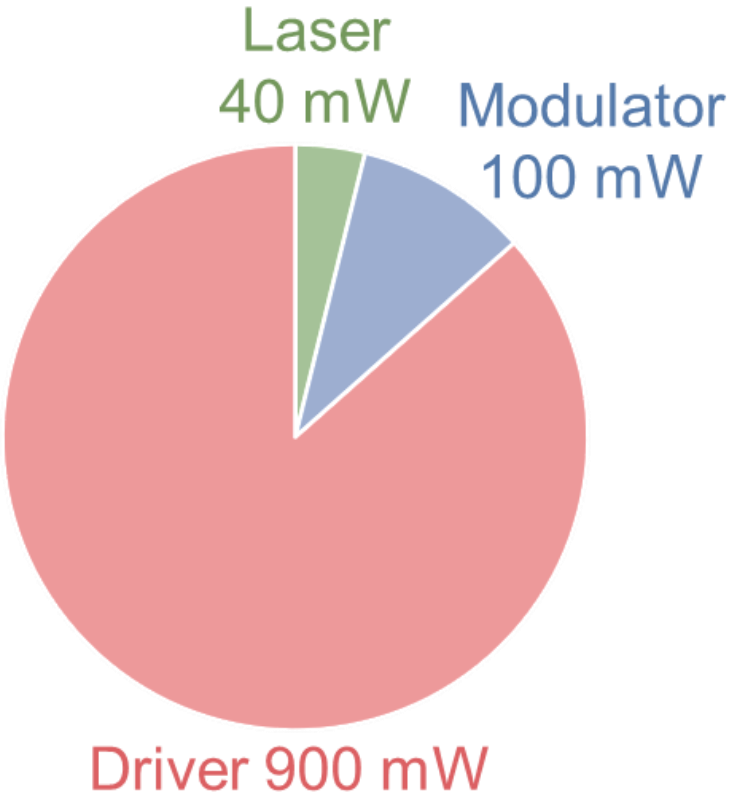
Power Breakdown of MZM-based Tx

Multi-Tbps drives massive parallelism, requiring **compact & low-power** Tx

MZM and Driver consume most power



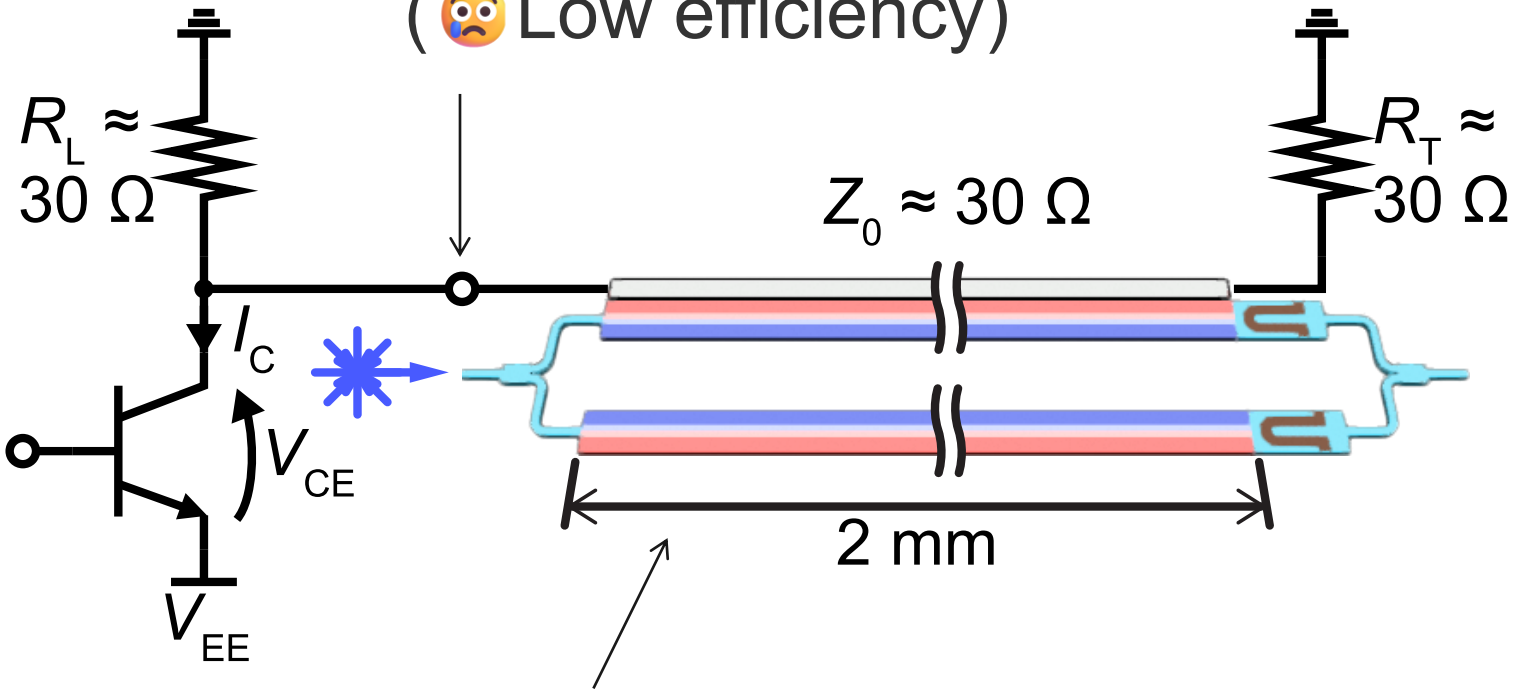
😢 **>1 W in Total (~10pJ/bit)**



Causes of Large Footprint and Low Efficiency

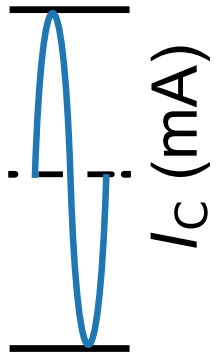
Low node impedance due to terminations

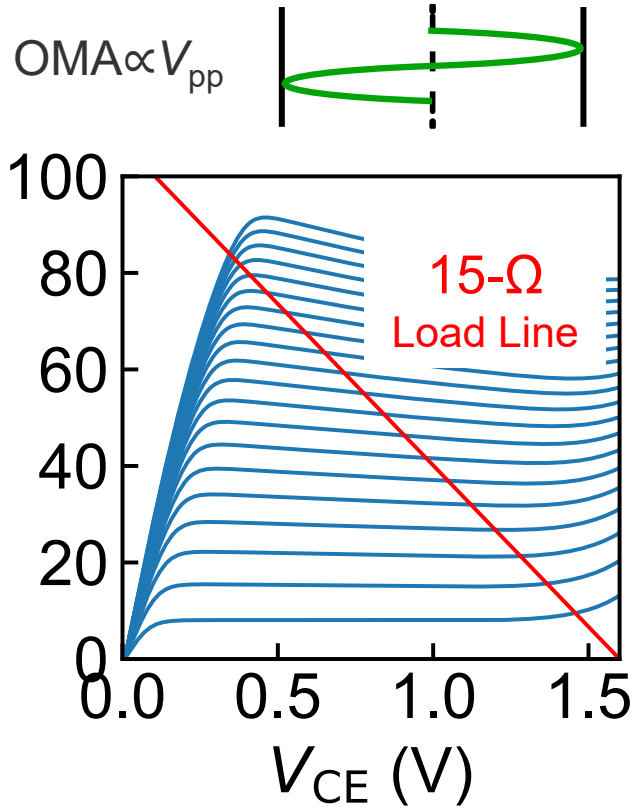
(😢Low efficiency)



Rib waveguide phase shifters

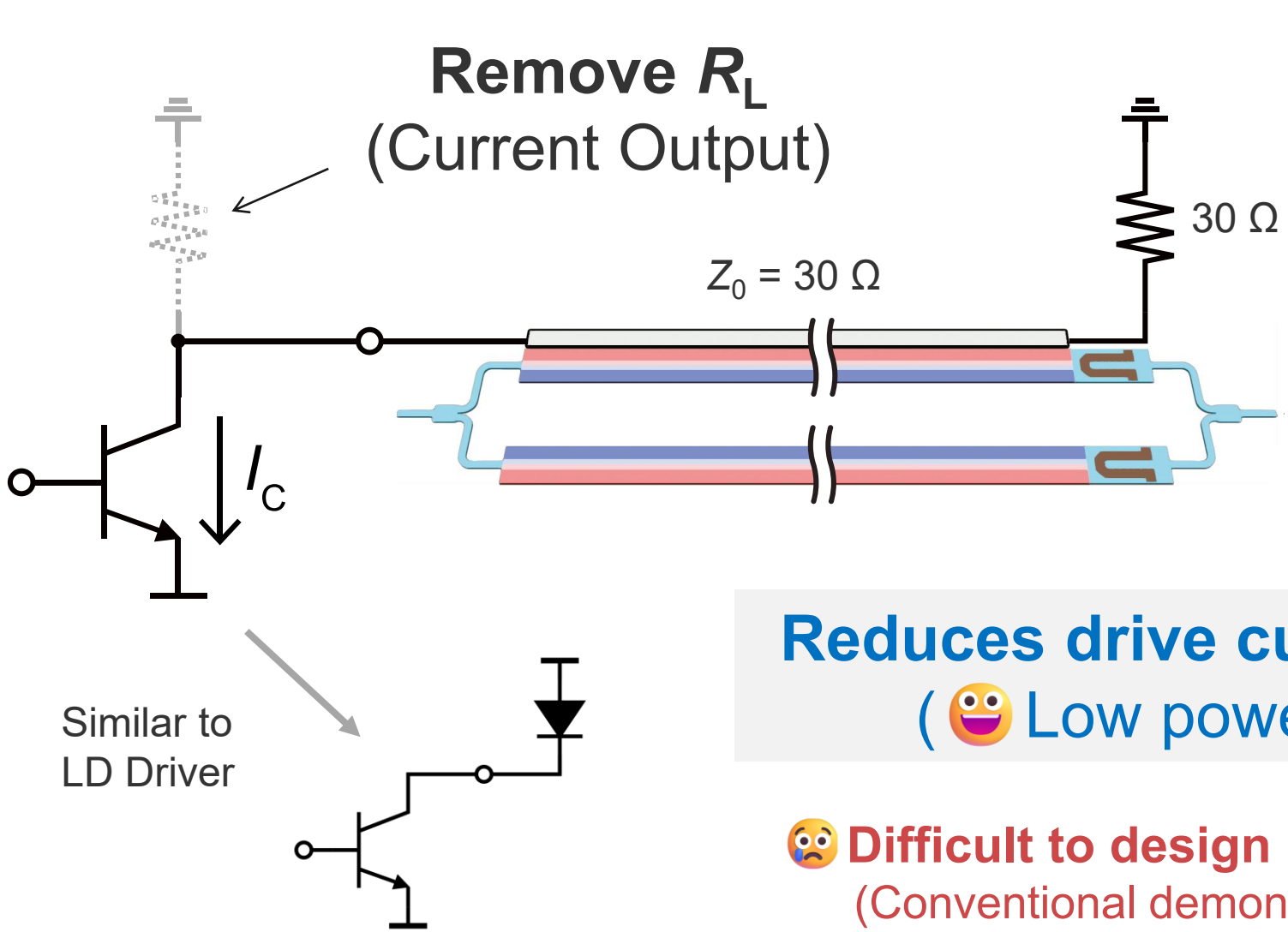
(😢Large Footprint)



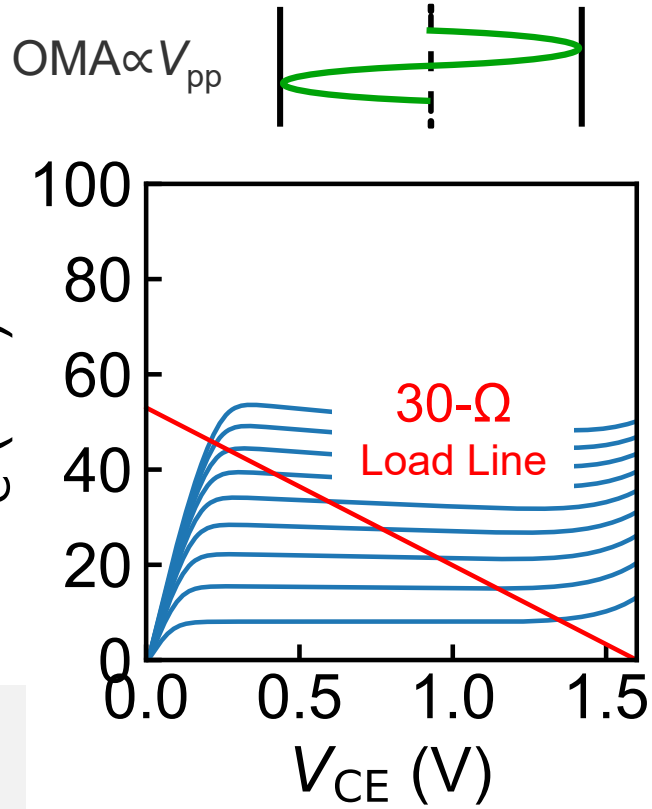


Open-Collector Driver

A. Giuglea *et al.*, *JLT*, 40(7), pp. 2080–2086 (2022).





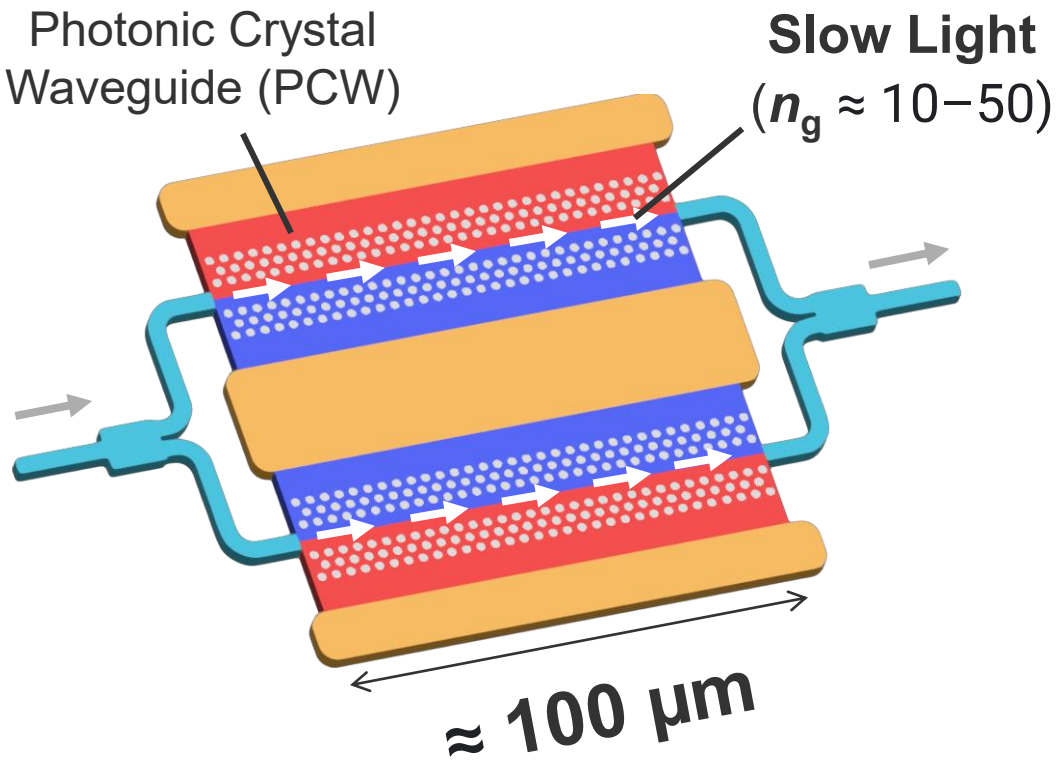


Reduces drive currents
(😀 Low power)

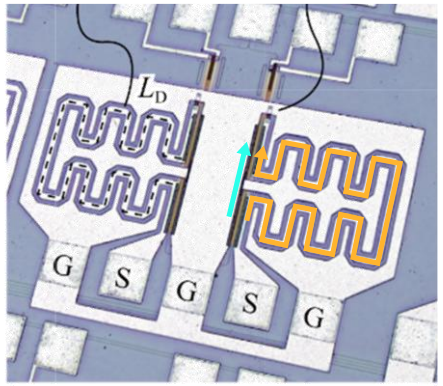
😢 **Difficult to design due to impedance mismatch**
(Conventional demonstration shows only <40 Gbps)

Si Photonic Crystal Slow-Light MZM

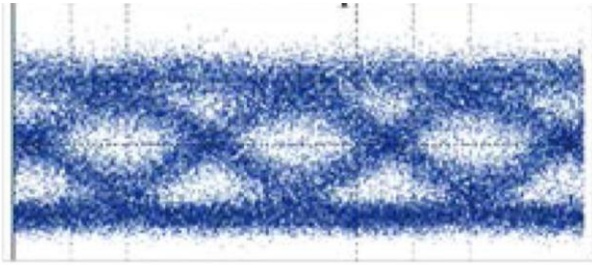
Modulation Efficiency ∝ n_g



64-Gbps by EO phase matching

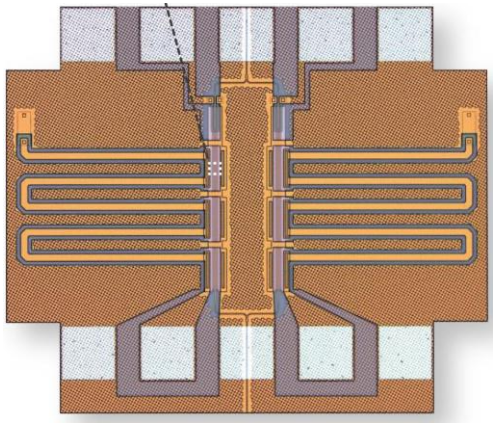


64 Gbps, 2.4 pJ/bit

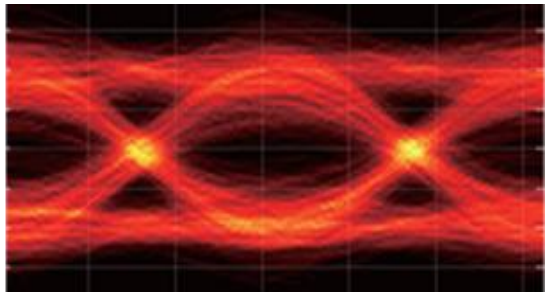


Y. Hinakura *et al.*, *IEEE JSTQE*, **27(3)**, 2021.

59-fJ/bit by impedance engineering



V_{pp} < 1 V, 59 fJ/bit

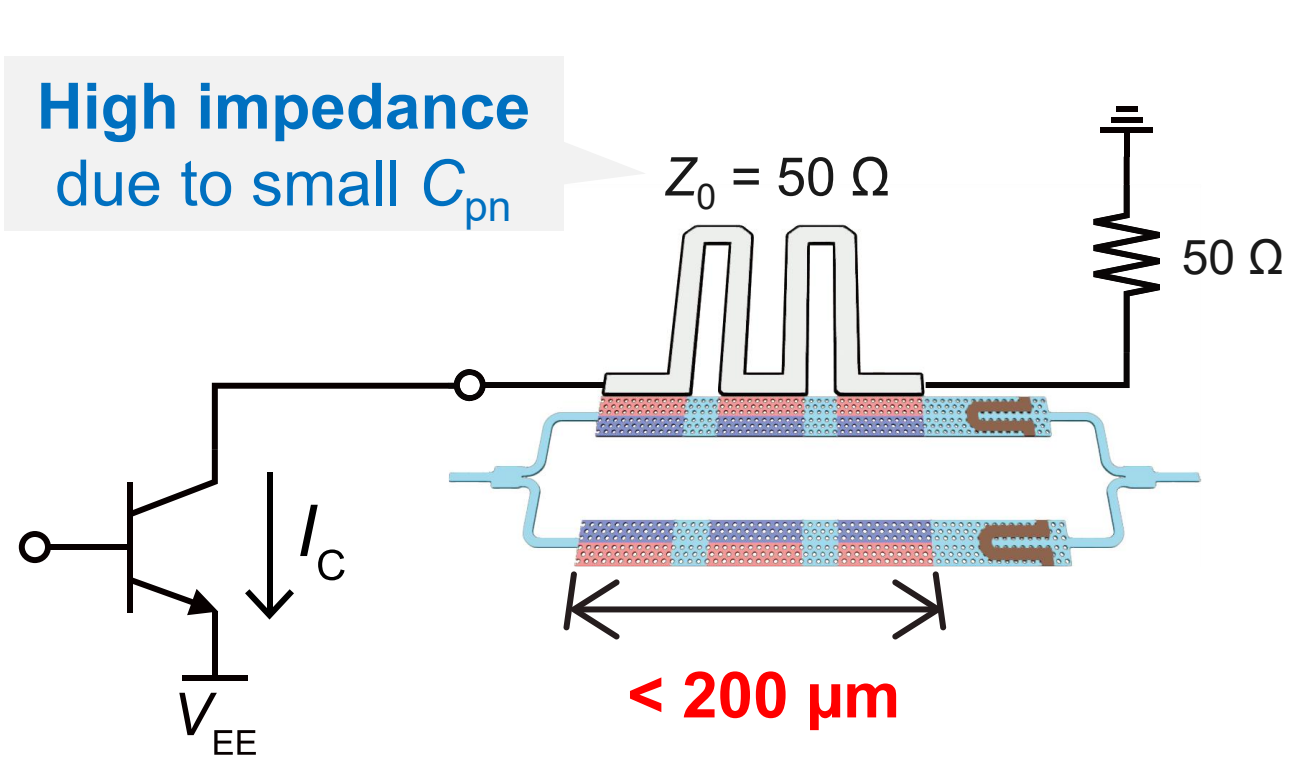


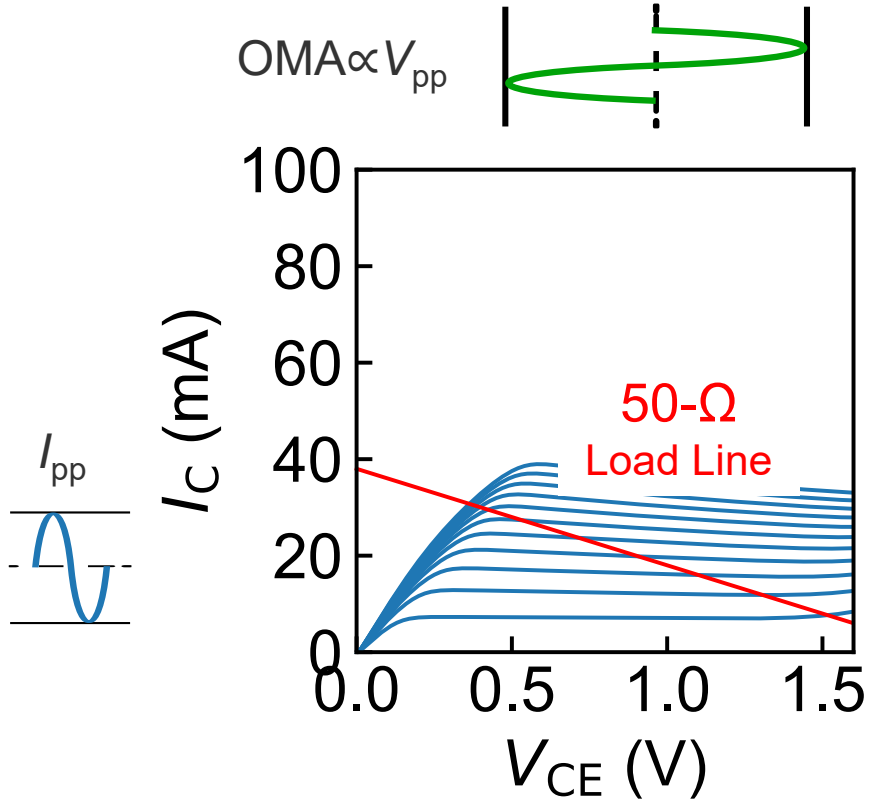
K. Kawahara *et al.*, *Optica*, **27(3)**, 2024.

Driver power not considered, but still dominant

Proposed EO-Converged Transmitter

Si PCW MZM + Current-Mode Driver → Small Footprint & High Efficiency





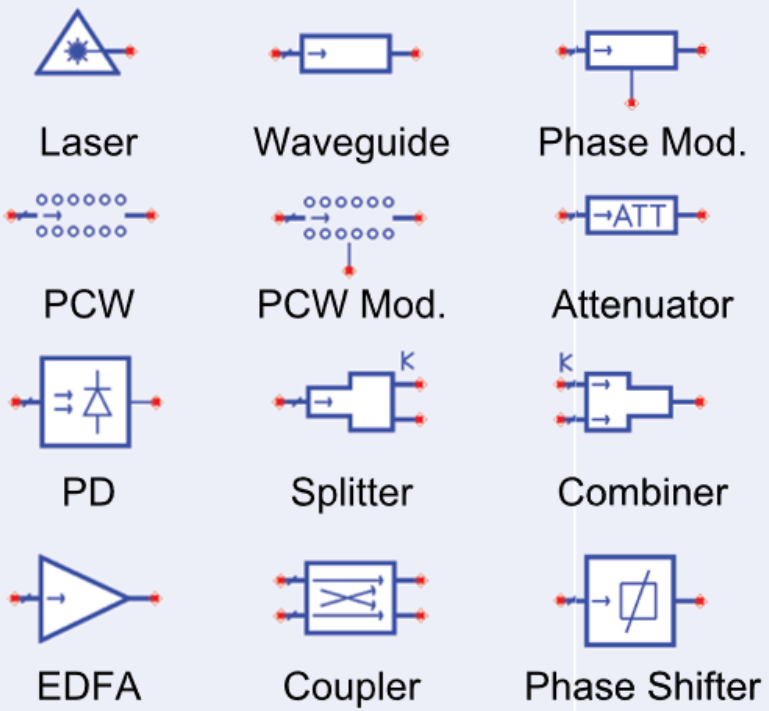
💡 To handle difficult current-mode design, we adopt **EO co-design**

EO Co-Design

K. Kawahara *et al.*, *IEEE J. Microwaves*, 2025 (Early Access).

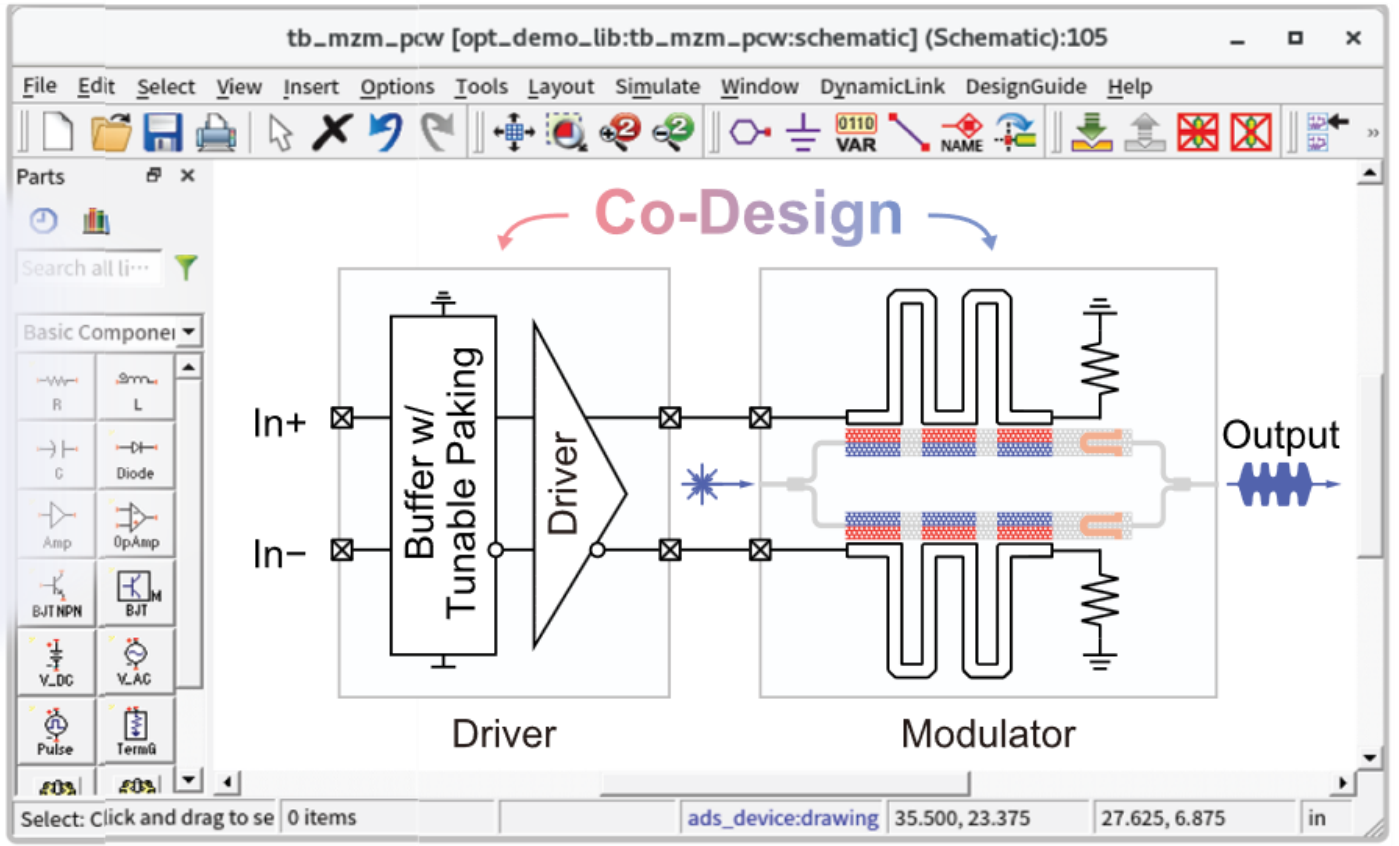
Photonic model library for standard electronic circuit simulators

In-House Photonic Model Library (Verilog-A)



Import

Industry Standard Electronic Circuit Simulator

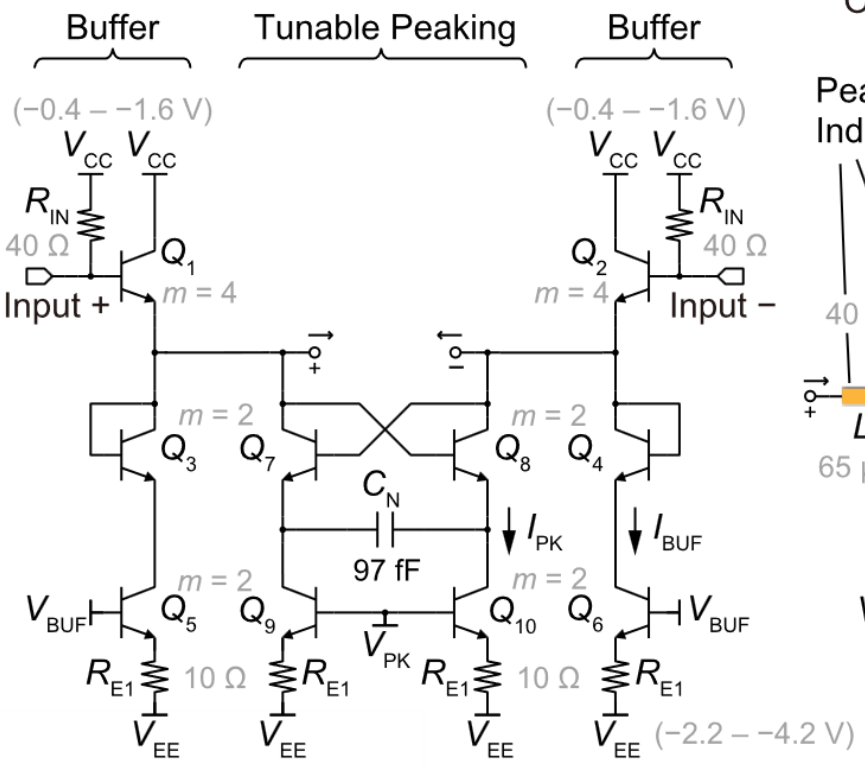


Now available on GitHub https://github.com/keikawa/Verilog-A-photonic-model-library

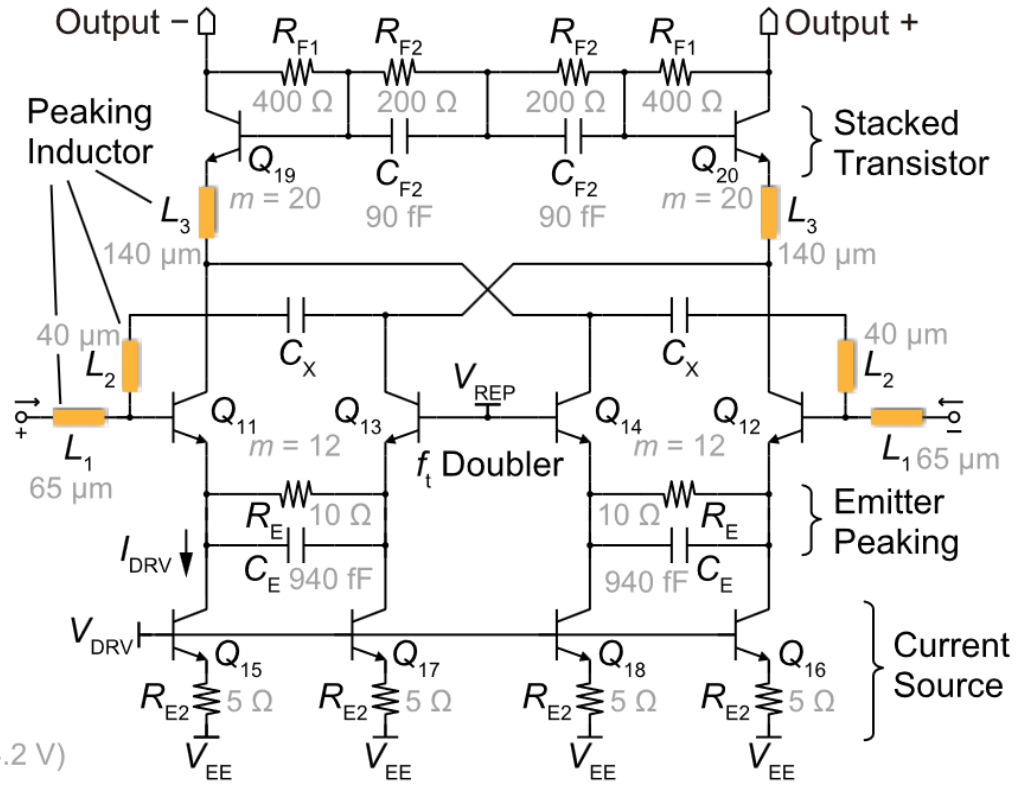
Driver Circuit

All parameters were optimized through co-simulation

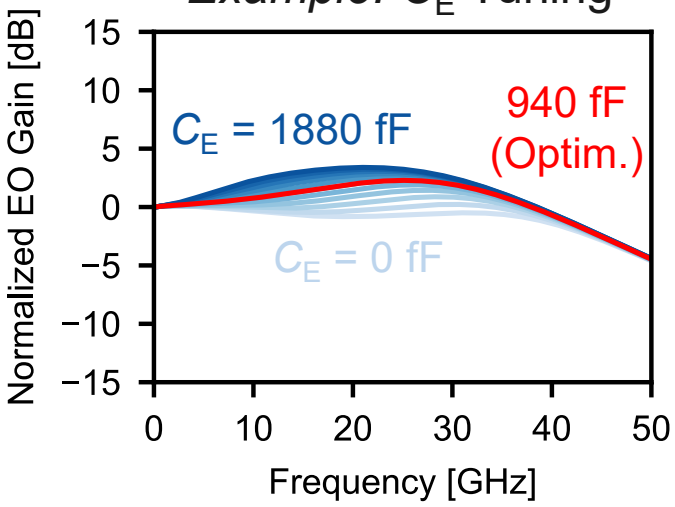
Input Buffer & Tunable Peaking



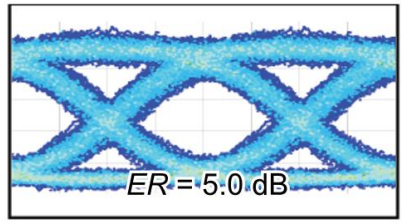
Open-Collector f_t-Doubler Driver



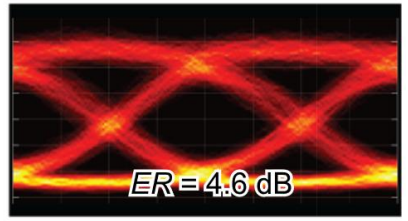
Example: C_E Tuning



Sim.

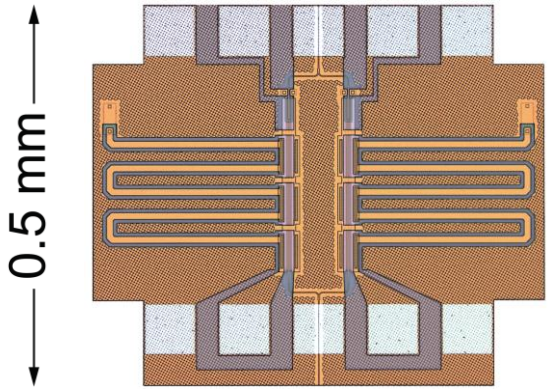


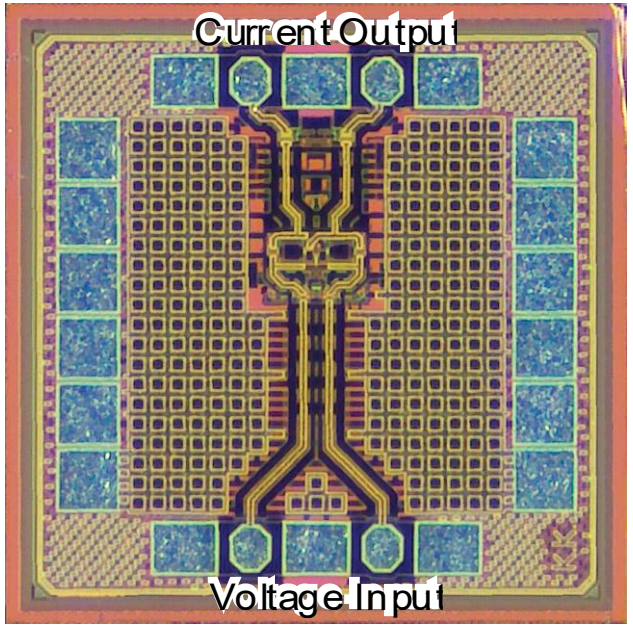
Meas.



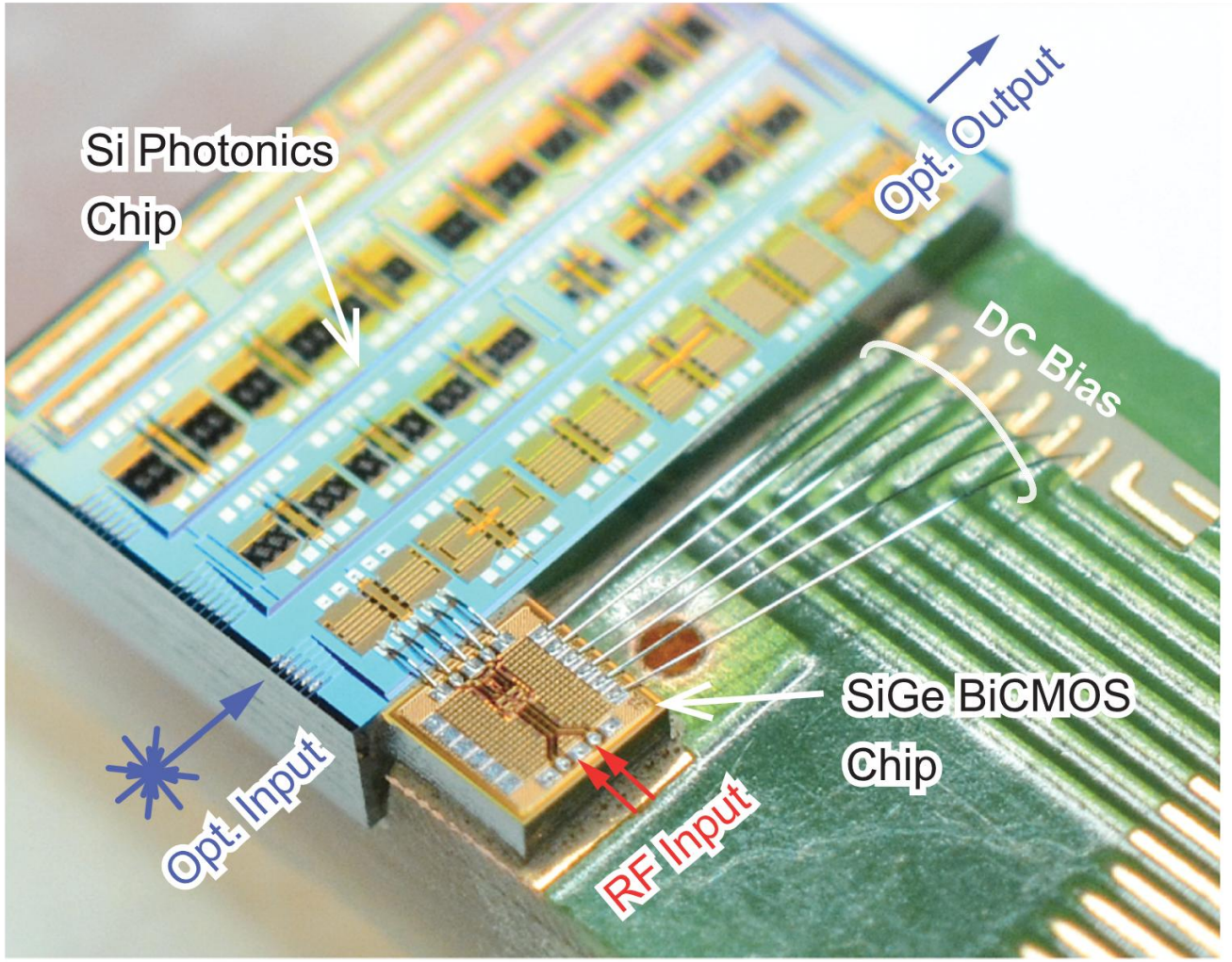
Fabricated Transmitter

Si Photonics (300-mm SOI Wafer)





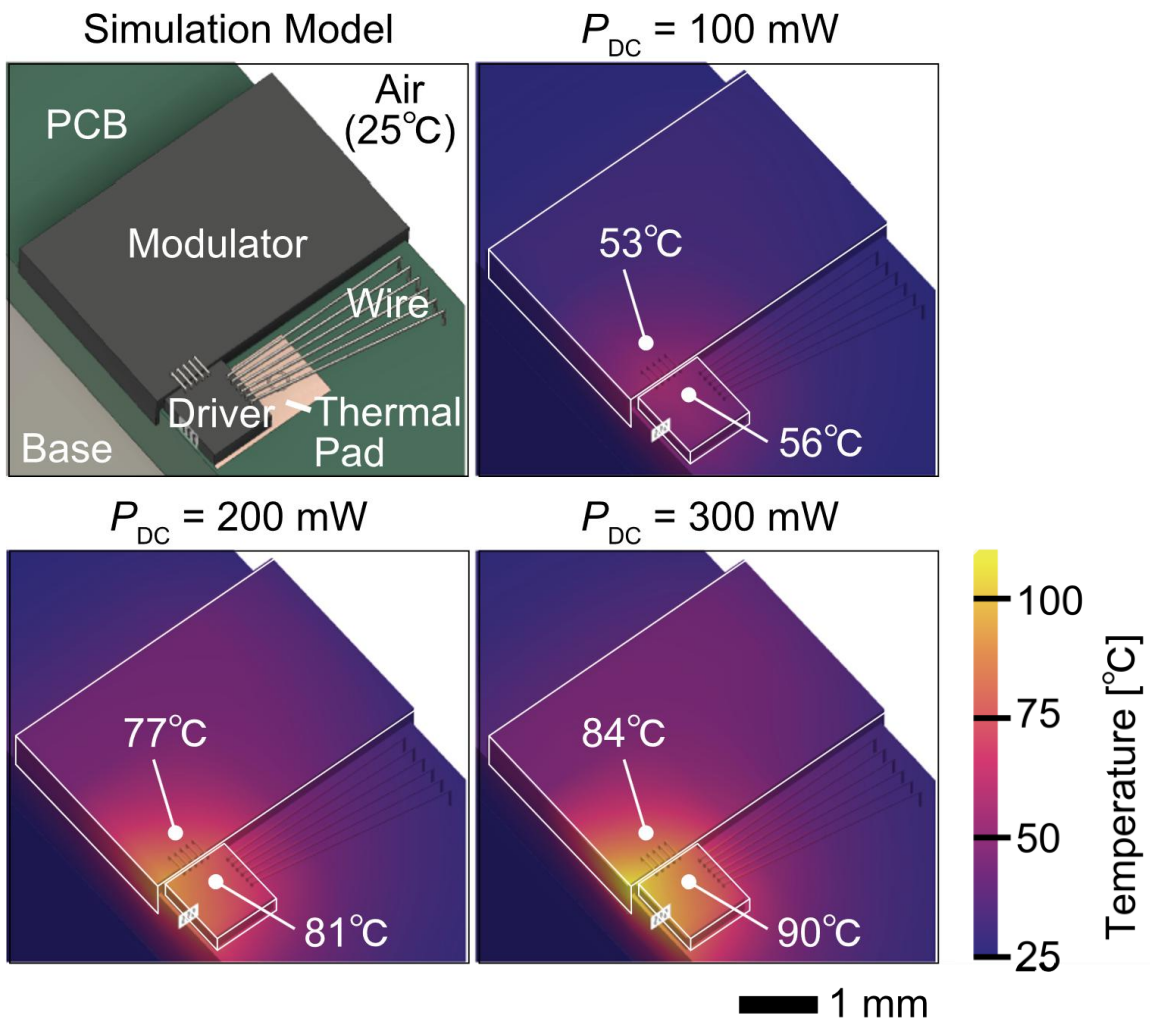
130-nm SiGe BiCMOS



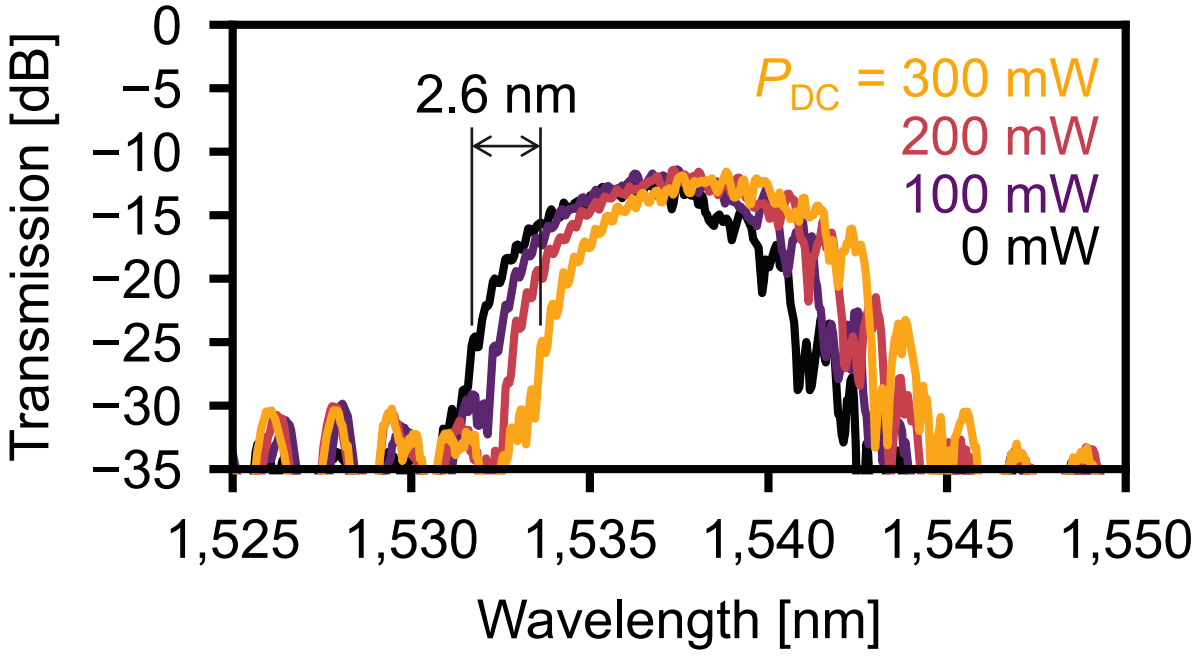
Active Footprint = 0.66 mm^2

Thermal Stability

Thermal Simulation



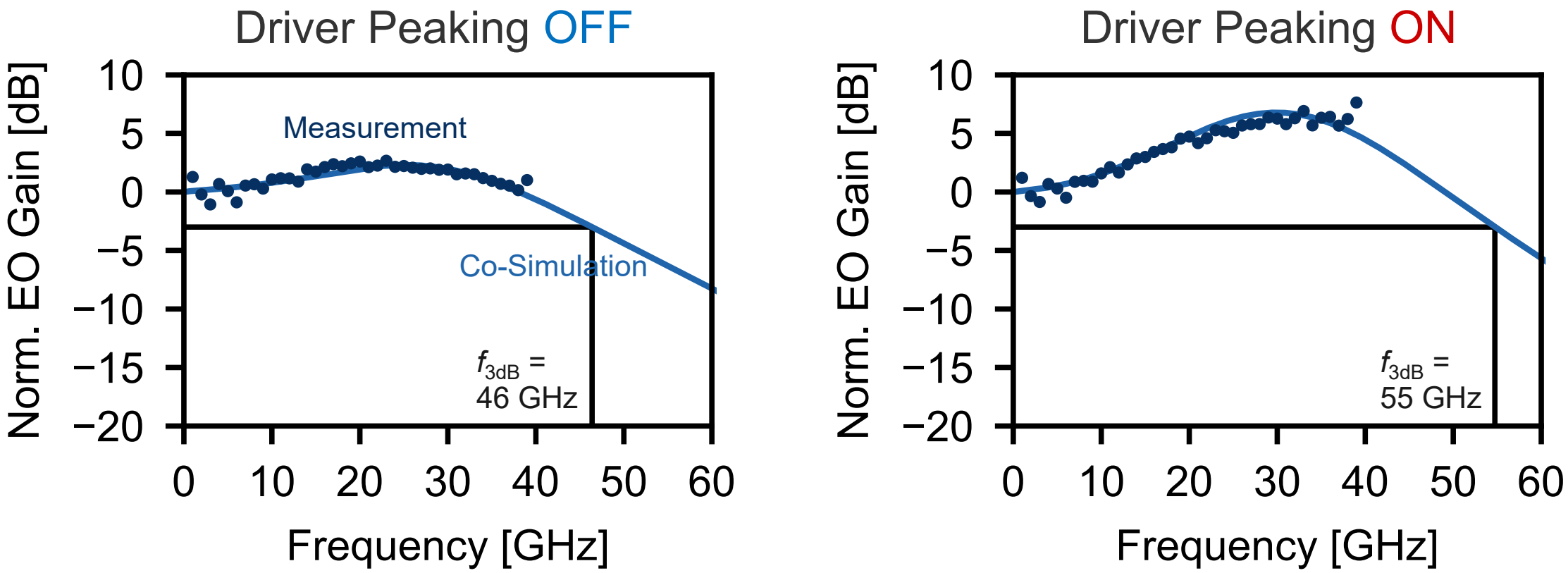
Optical Transmission Spectrum



No wavelength/temperature control required

35-nm bandwidth (n_g = 20) can be designed by optimizing the PCW structure. Hirotani *et al.*, *CLEO PR*, 2022.

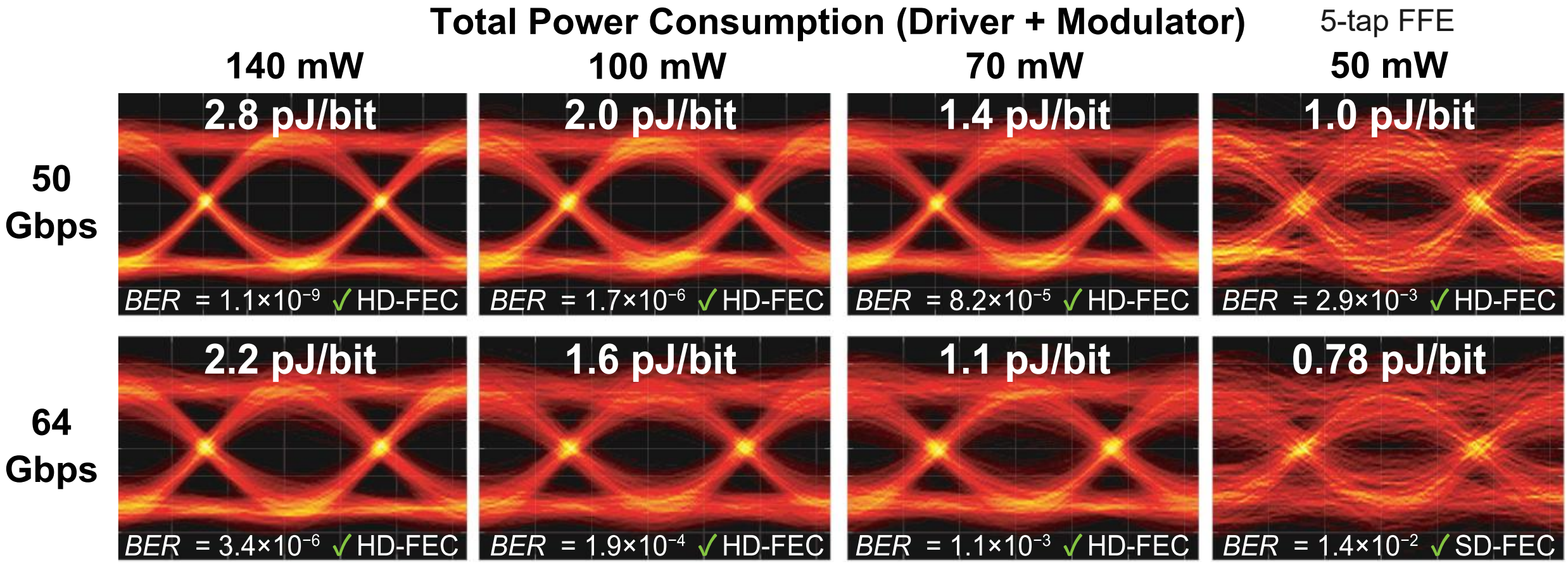
EO Frequency Response



Measurements agree well with the co-simulations

f_{3dB} exceeding 50 GHz, 100 Gbaud operation is expected

Signal Transmission Results



Signal transmission achieved with low power consumption below 100 mW

Best Efficiency (SD-FEC) **= 0.78 pJ/bit**

Conclusion

Low-power & Compact MZM-based Tx

- ✓ **50-mW** Total Power (**0.78 pJ/bit**)
- ✓ **0.66-mm²** Active Footprint
- ✓ **55-GHz** EO Bandwidth
- ✓ **Thermally Stable**

Efficient & small device enables **massive parallel** SiPh interconnects

