YNU
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59-fJ/bit Si Photonic Crystal Slow-Light Modulator with FinFET-Compatible Driving Voltage

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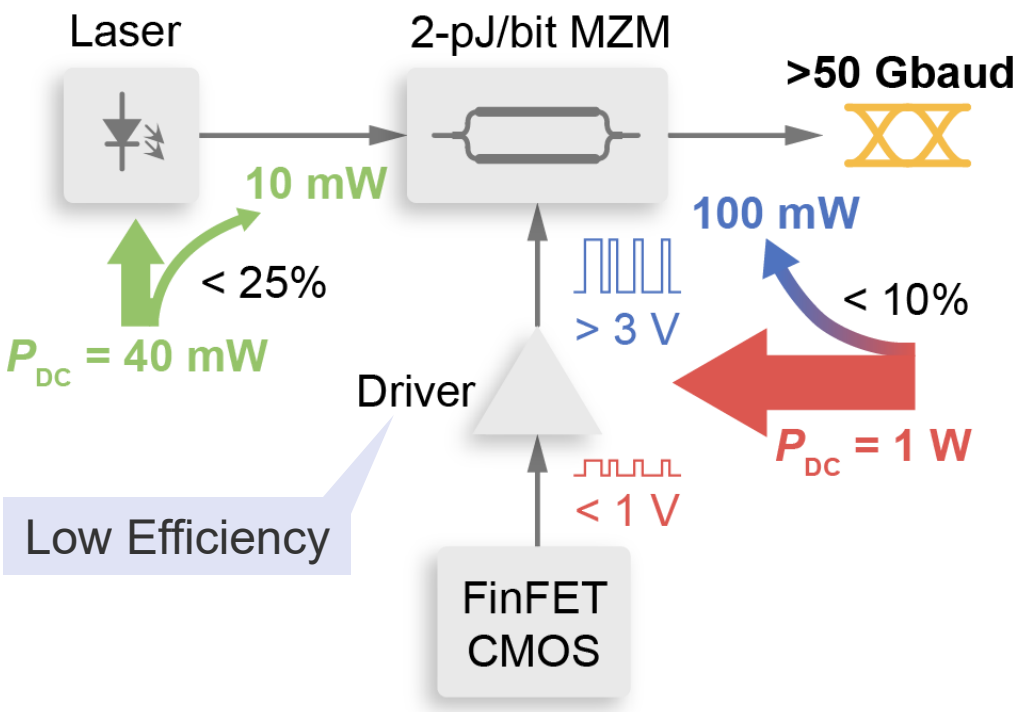
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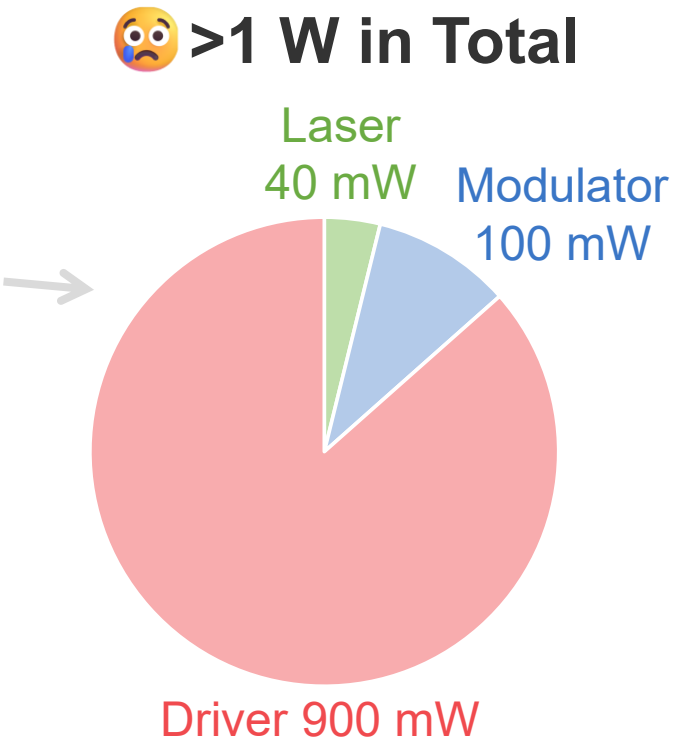
Background: Optical Interconnects

Significant increase in energy use in data centers and HPC

Necessity for high-efficiency SiPh transceivers

In SiPh transmitters, modulators and drivers consume most power



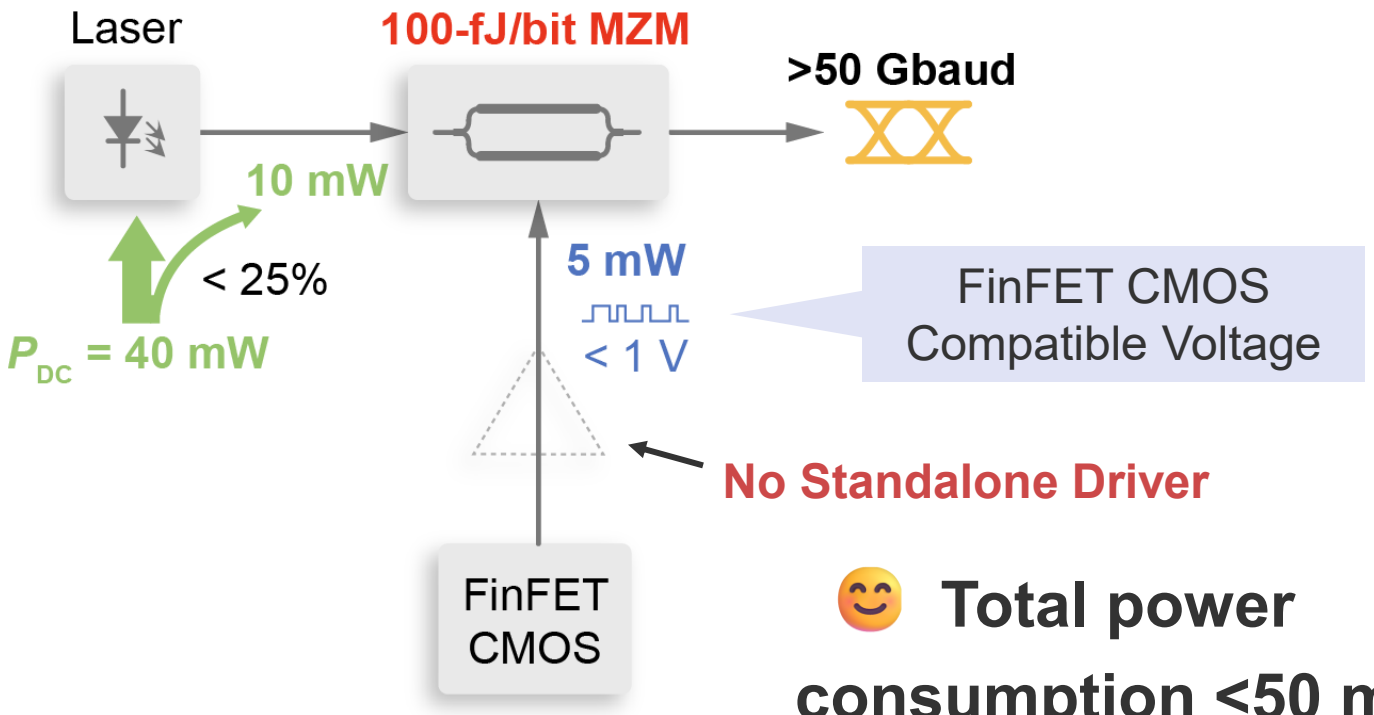


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Significant increase in energy use in data centers and HPC

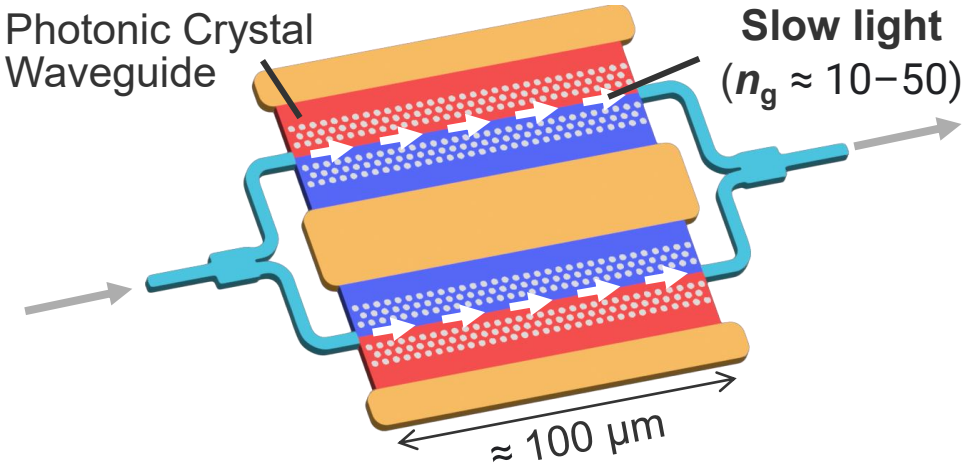
Necessity for high-efficiency SiPh transceivers

If modulator's efficiency is improved to **100 fJ/bit** ...



😊 **Total power consumption <50 mW**

Si Slow-Light MZM

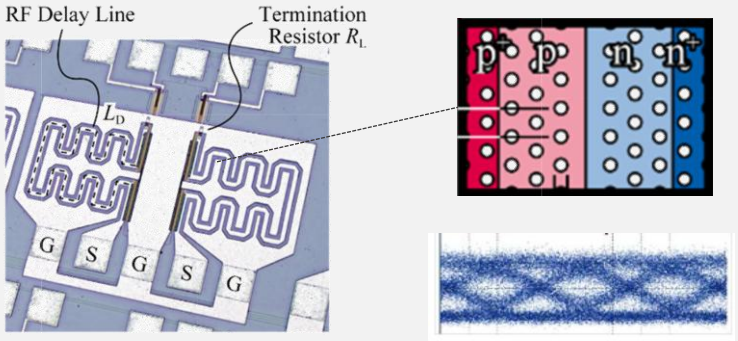


Modulation efficiency $\propto n_g$

- 😊 Small footprint (≈ 100 μm)
- 😊 High speed (>64 Gbaud)
- 😢 High driving voltage (>3 V)

Yokohama National Univ., 2021

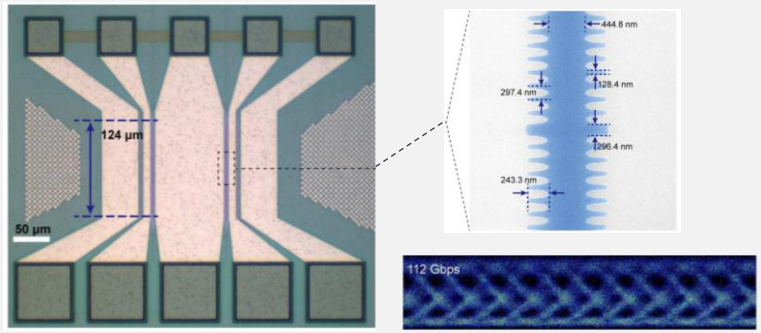
64 Gbaud V_{pp} **= 3.5 V**



Y. Hinakura et al., IEEE JSQTE., **27** (2021).

Peking Univ., 2023

112 Gbaud V_{pp} **= 5.0 V**

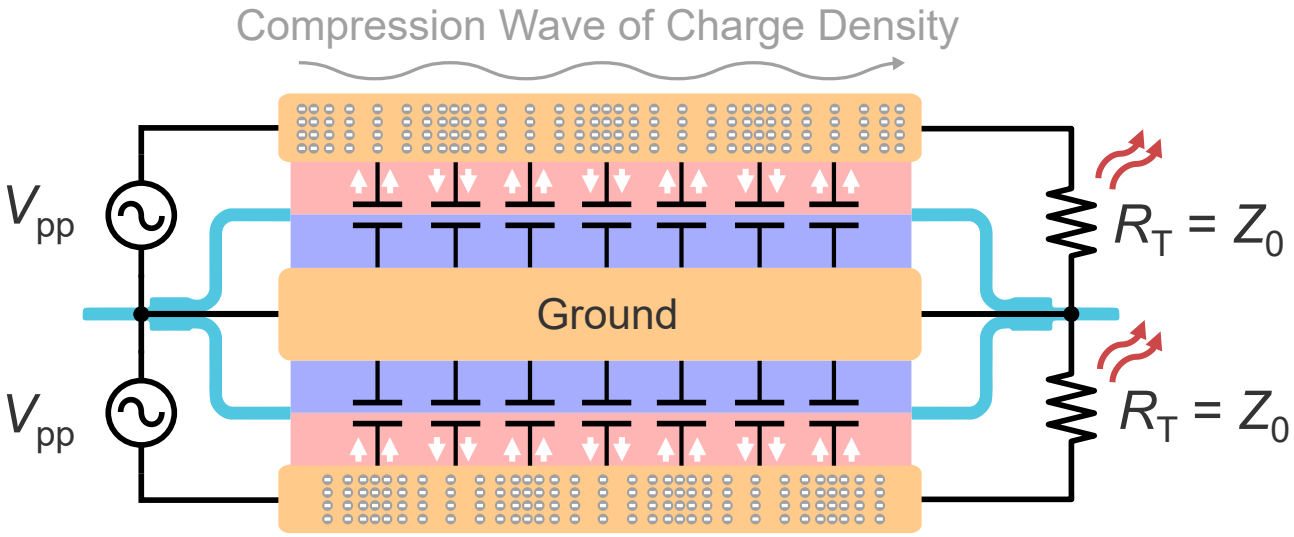


C. Han et al., Science Advances **9** (2023).

Bit energy is still limited to several pJ/bit

Challenges to High Efficiency

Most power is consumed by the termination resistor in traveling-wave electrodes



Power Consumption

$$P_{RF} = \frac{V_{pp}^2}{4R_T}$$

To reduce the power consumption, we need to

① Increase R_T, but Z_0 is typically **30 Ω** due to large C_{pn}

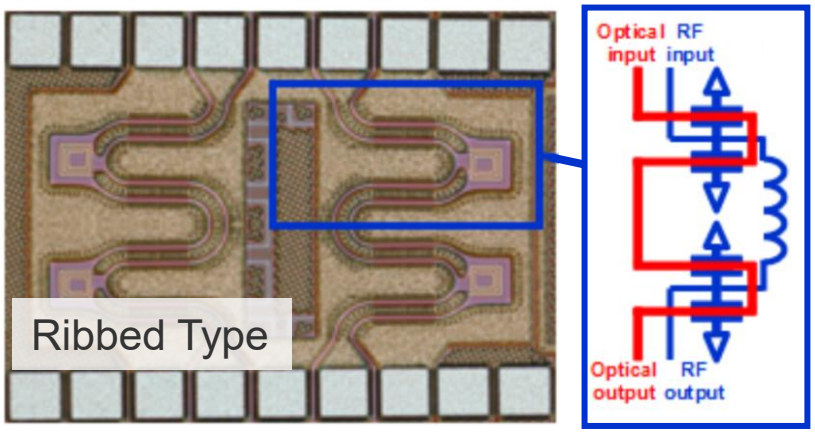
② Decrease V_{pp}, but long phase shifter or large n_g causes **EO phase mismatch**

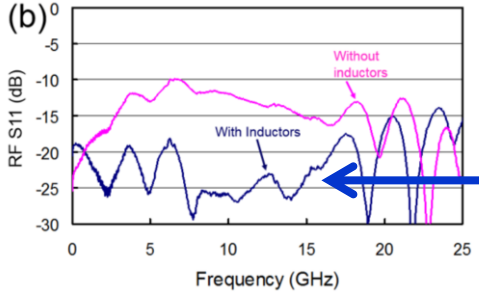
High impedance and EO phase matching are critical challenges

RF Design in Si MZMs

High Impedance

Distributed Electrode（IBM, 2015）





LC Ladder with Inductors

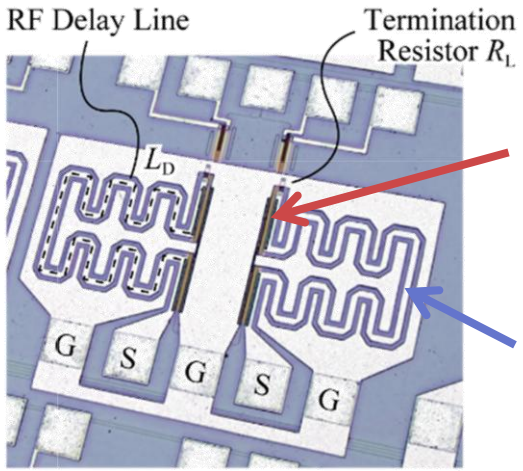
50 Ω

D. M. Gill et al., Opt. Express, **23** (2015).

😢 Large RF Loss
😢 Degraded Phase Matching

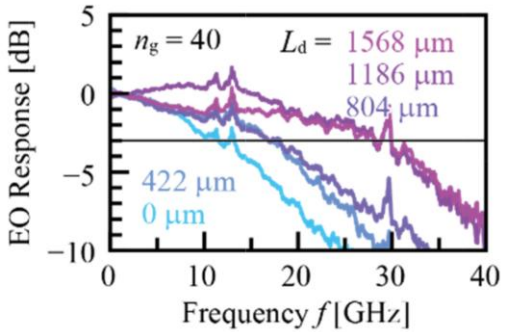
EO Phase Matching

Meander Line Electrode（YNU, 2018–）



Slow-light Phase Shifter

RF Delay Line

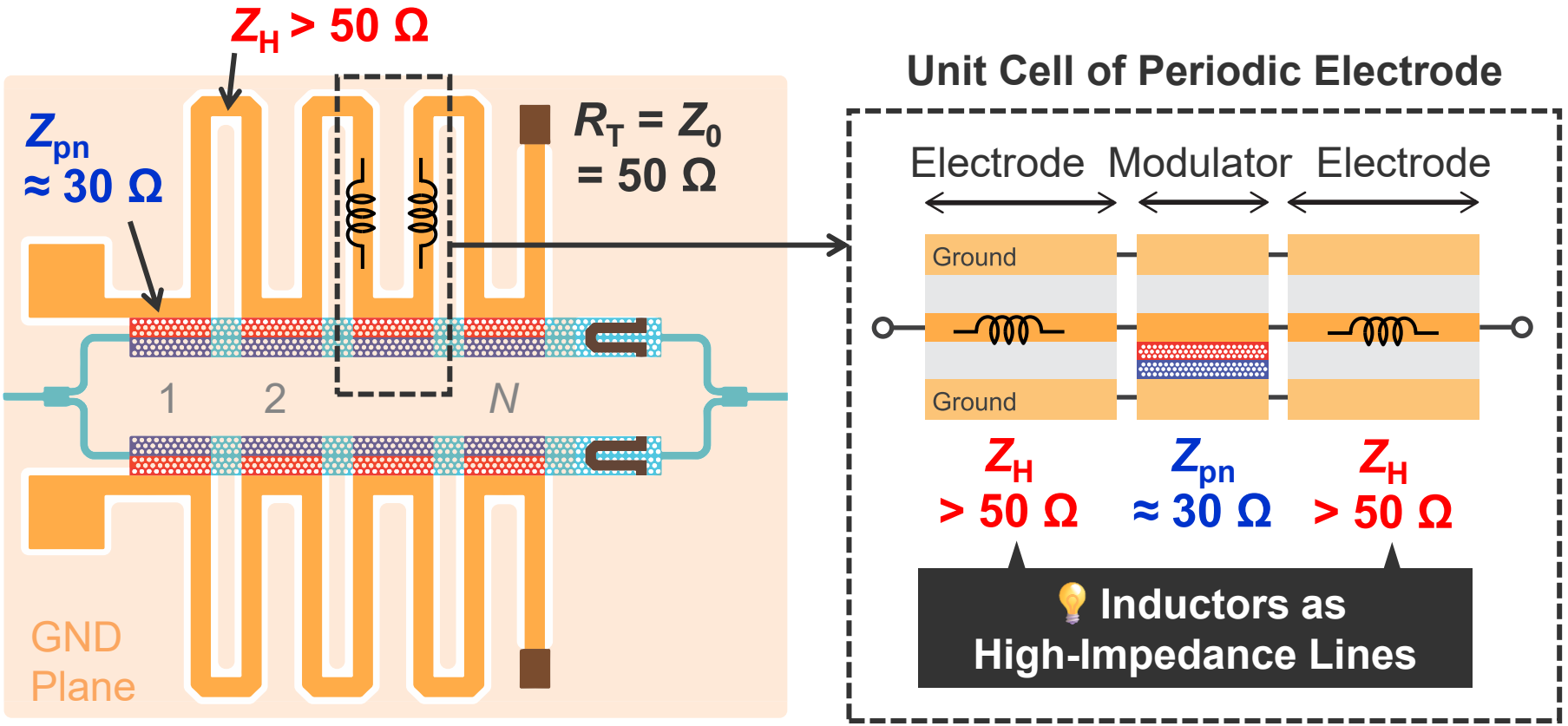


Y. Hinakura et al., IEEE JSQTE., **27** (2021)..

😢 Low Impedance

Distributed Electrode Slow-Light MZM

Periodic electrodes with segmented phase shifters and high-Z lines ($Z_H > Z_0$)

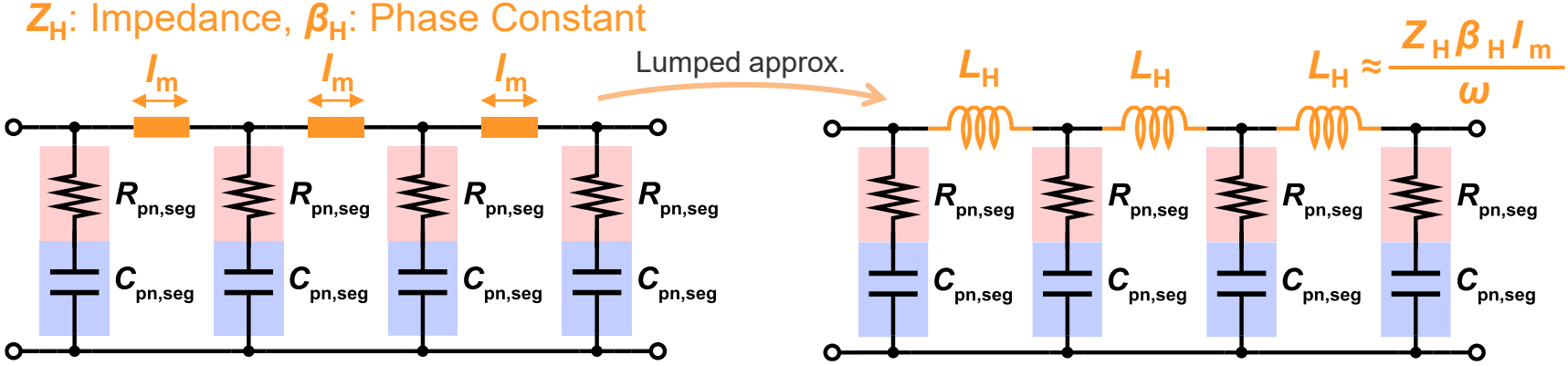


① **High impedance** and ② **EO phase matching** under low RF loss

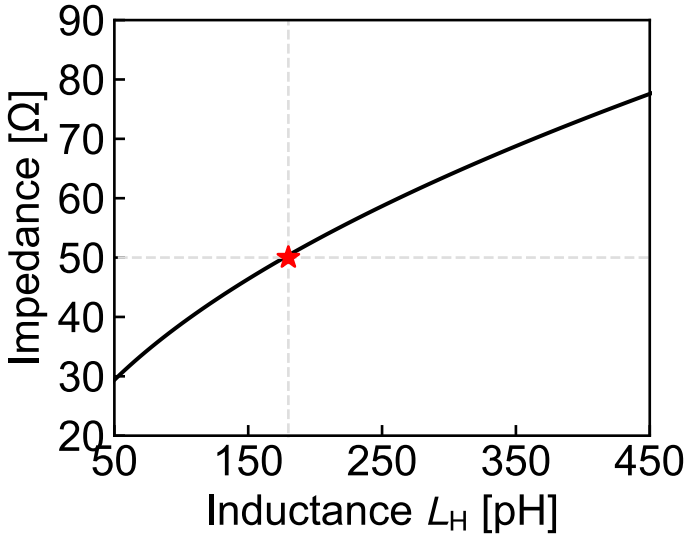
① High Impedance

Line inductance and C_{pn} form a LC ladder like a distributed constant circuit

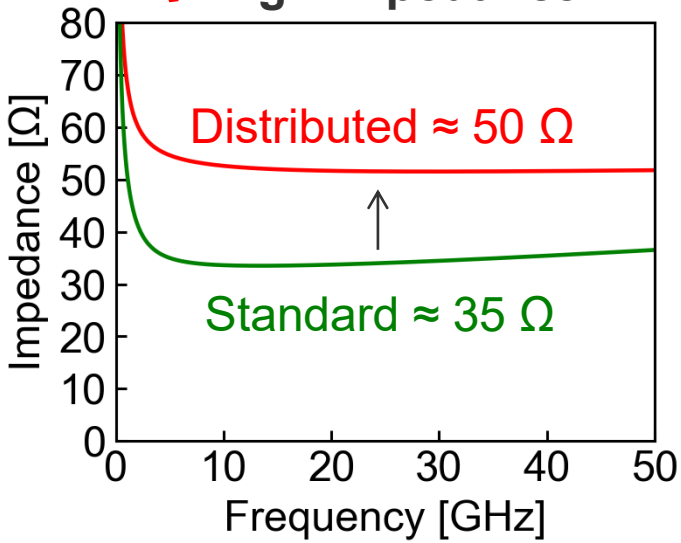
Z_H: Impedance, β_H: Phase Constant



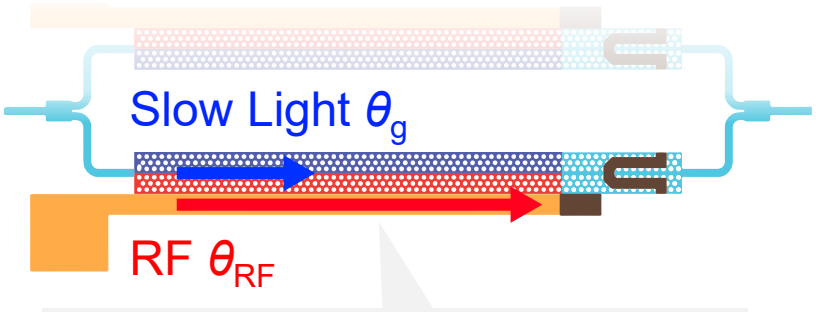
L_H increases Z_0



✓ High Impedance

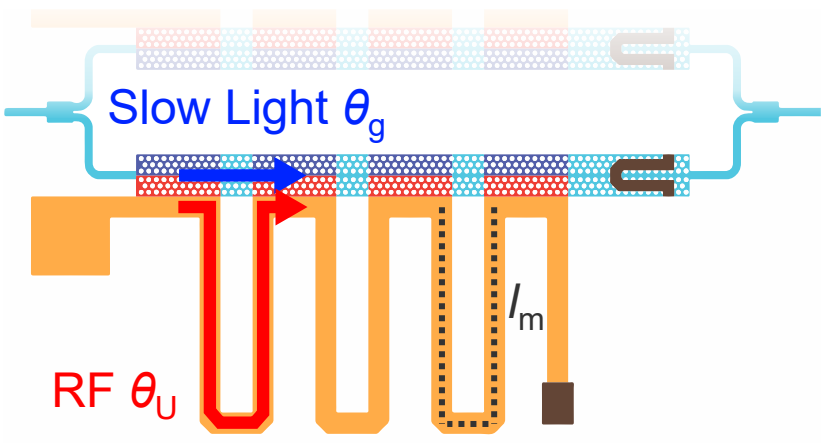


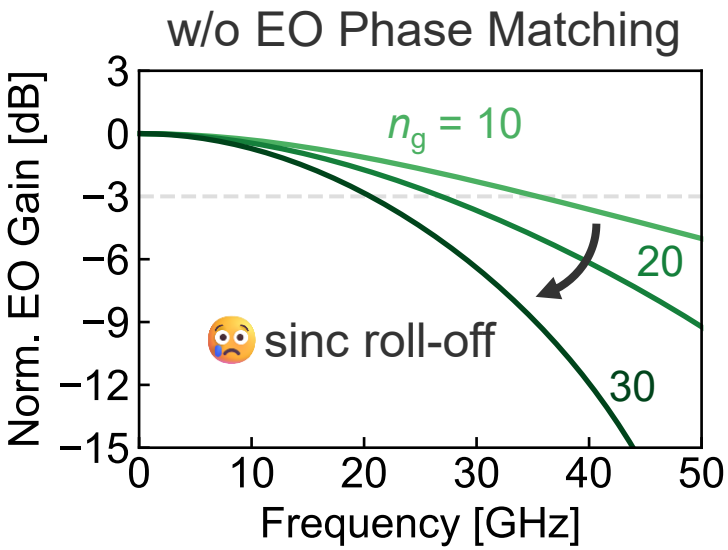
② EO Phase Matching

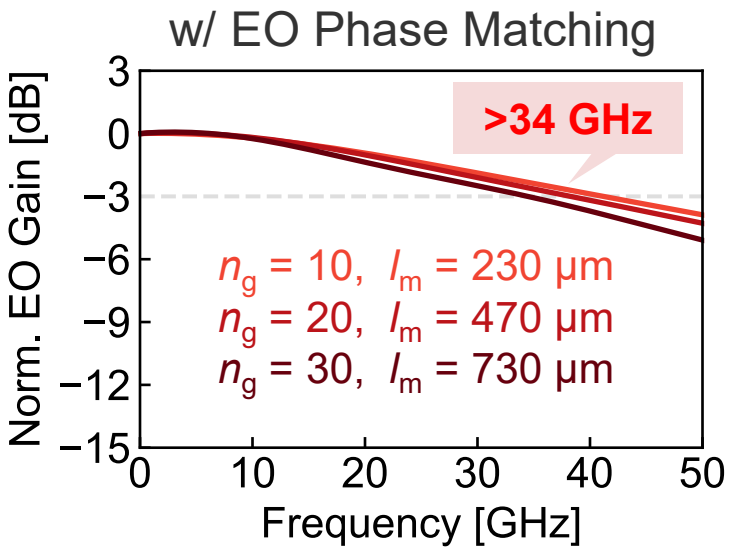


Roll-off due to phase mismatch

$\eta(f) = \mathrm{sinc}[(\theta_g - \theta_{RF}) / 2]$



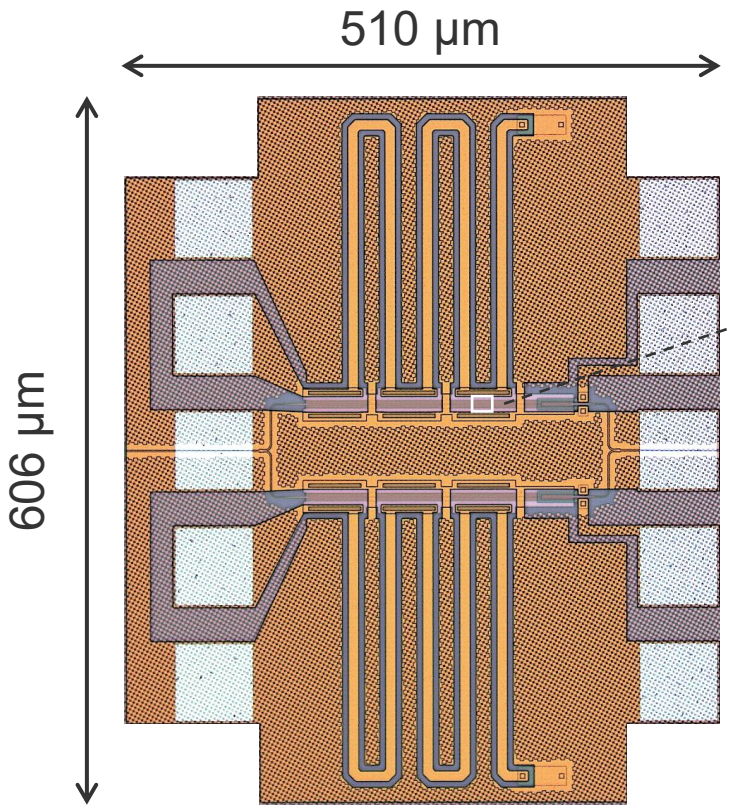


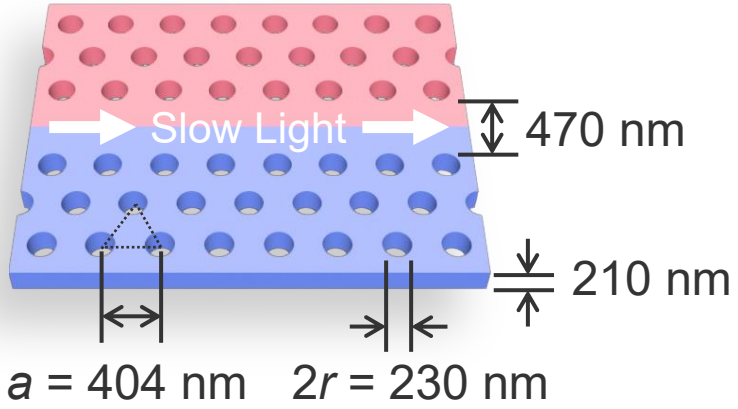


✓ Increasing n_g and reducing driving voltage while maintaining EO bandwidth

Prototype Modulator

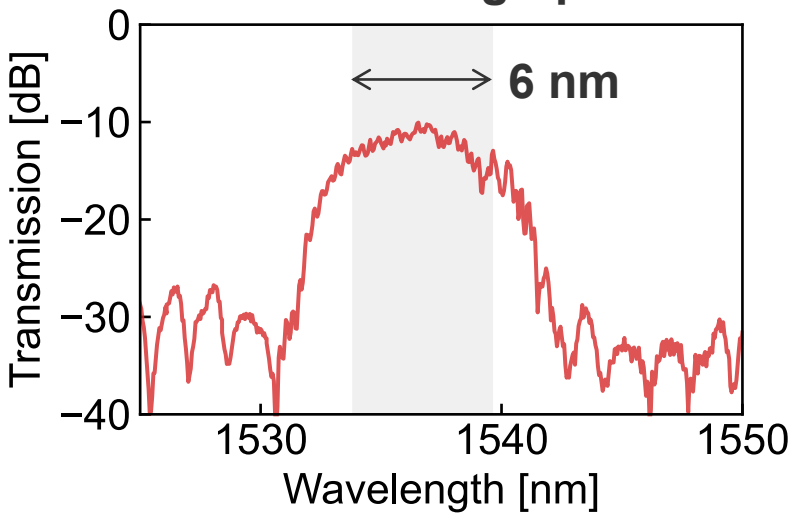
Fabricated using a CMOS-compatible 300-mm SOI wafer process



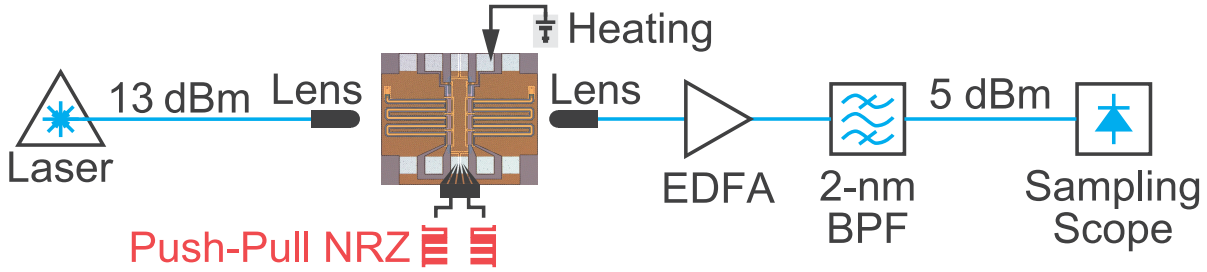


✓ **0.3-mm² Small Footprint**

✓ **Wide Working Spectrum**



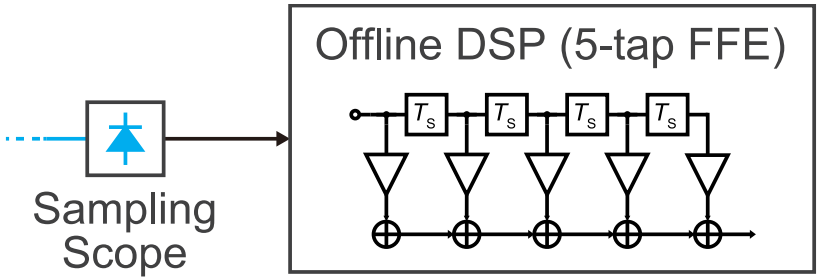
DSP-Free Signal Transmission

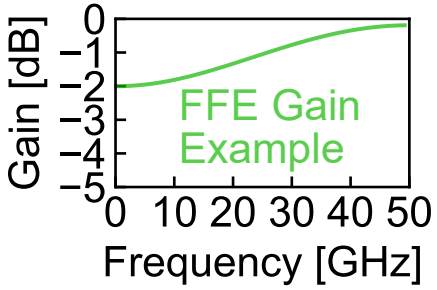


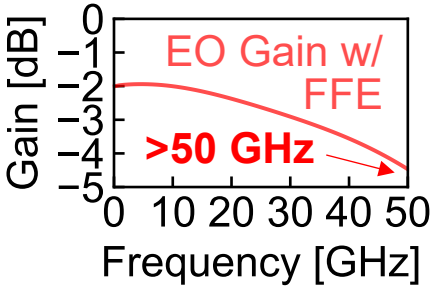
	V_{pp} = 2.2 V	1.6 V: FinFET IO	0.87 V: FinFET Core
50 GBd	493 fJ/bit *ER*: 4.5 dB, *ML*: 6.3 dB *BER* = 1.6×10^{-5} (✓HD-FEC)	246 fJ/bit *ER*: 3.0 dB, *ML*: 6.8 dB *BER* = 2.0×10^{-4} (✓HD-FEC)	76 fJ/bit *ER*: 2.0 dB, *ML*: 7.1 dB *BER* = 2.3×10^{-3} (✓HD-FEC)
64 GBd	385 fJ/bit *ER*: 4.1 dB, *ML*: 6.4 dB *BER* = 5.9×10^{-3} (✓SD-FEC)	193 fJ/bit *ER*: 2.8 dB, *ML*: 6.8 dB *BER* = 1.1×10^{-2} (✓SD-FEC)	59 fJ/bit *ER*: 1.8 dB, *ML*: 7.2 dB *BER* = 2.4×10^{-2}

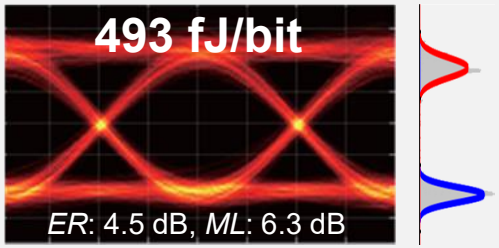
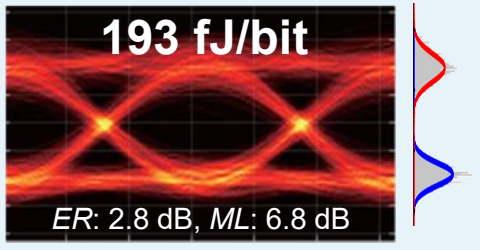
DSP-free transmission demonstrated up to 76 fJ/bit

Enhancing Symbol Rate w/ FFE







	V_{pp} = 2.2 V	1.6 V: FinFET IO	0.87 V: FinFET Core
50 GBd	 BER = 2.8×10^{-13} (✓Error Free)	 BER = 4.1×10^{-8} (✓HD-FEC)	 BER = 4.3×10^{-4} (✓HD-FEC)
64 GBd	 BER = 4.0×10^{-8} (✓HD-FEC)	 BER = 1.5×10^{-5} (✓HD-FEC)	 BER = 2.4×10^{-3} (✓HD-FEC)

Distributed electrodes w/ FFE offers the potential for >100 GBd

Conclusion

59-fJ/bit Si Photonic Crystal Slow-Light Modulator with FinFET-Compatible Driving Voltage

Purpose	Improve energy efficiency of optical modulators
Proposal	Distribute electrode slow-light Si MZM
Achievement	✓ **0.3-mm^2** small footprint
	✓ **50-Ω** flat impedance
	✓ **64-Gbaud** transmission with V_{pp} **= 0.87 V**
	✓ Energy efficiency of **59 fJ/bit**
	✓ **Potential for >100 GBd** with FFE