A 50 Gbps 49 mW CMOS Analog Multiplexer for a DAC Bandwidth Tripler

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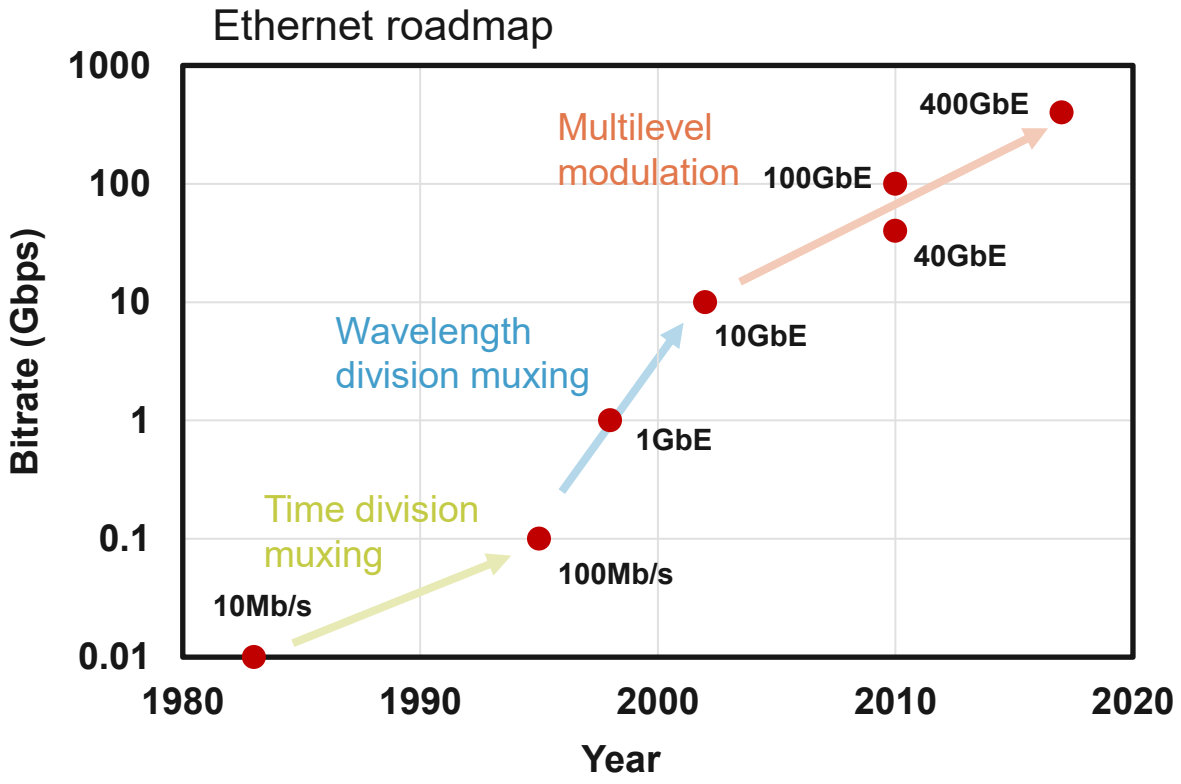
2022 IEEE Radio and Wireless Symposium (RWS 2022)

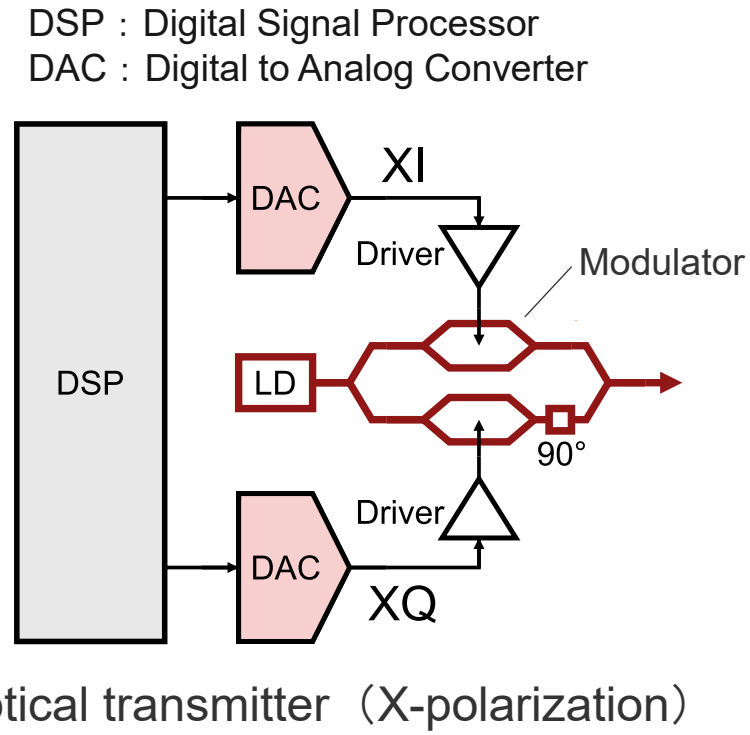
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Fiber-optic communications



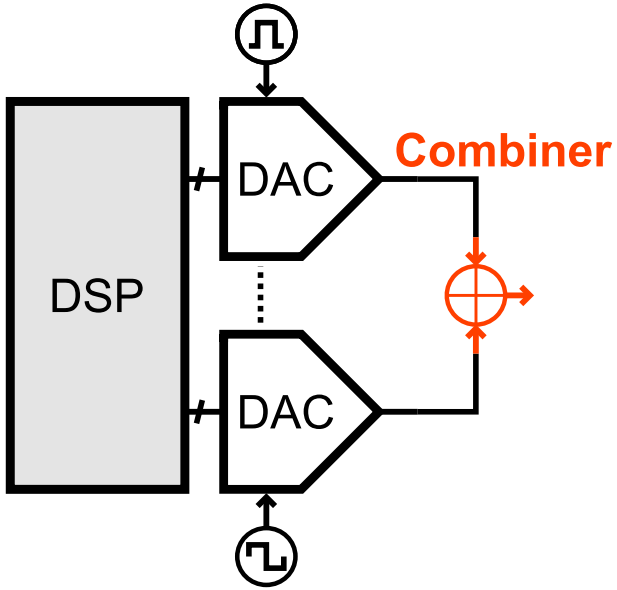


Optical transmitter（X-polarization）

- Multilevel modulation and digital signal processing
  →**High-speed digital-to-analog converters** are required !!

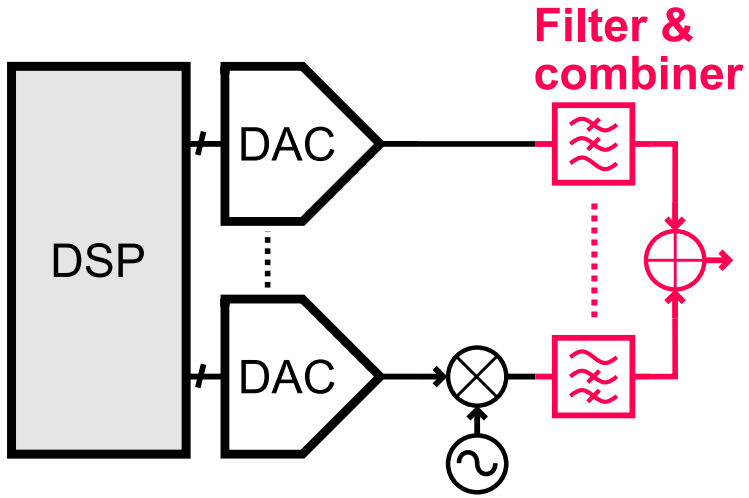
DAC interleaving concepts

Univ. of Stuttgart (2015)
Time interleaving



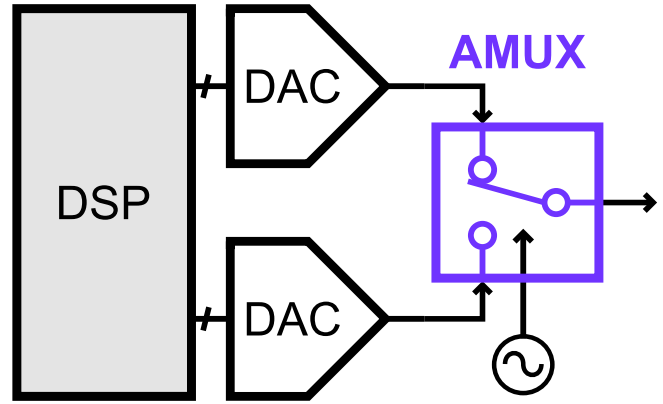
- 😄 Enhances sample rate
- 😥 No bandwidth enhancement

Nokia Bell lab. (2017)
Freq. interleaving



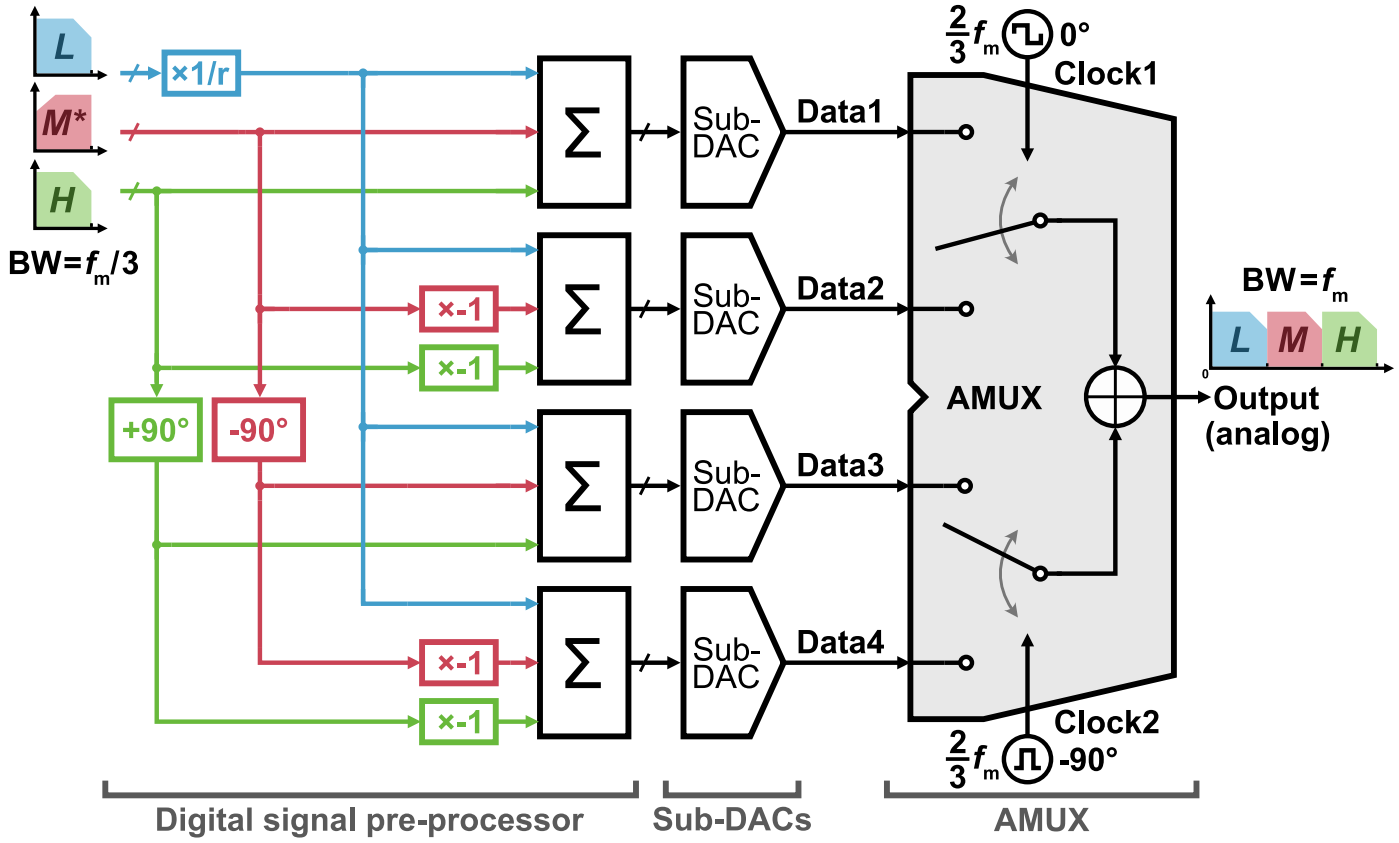
- 😄 Enhances bandwidth by *N*
- 😥 Requires analog filters
- 😥 Delay time mismatch

NTT lab. (2020)
Freq. interleaving
with an analog MUX



- 😄 Not require analog filters
- 😄 No delay time mismatch
- 😥 Bandwidth enhancement is limited up to doubling

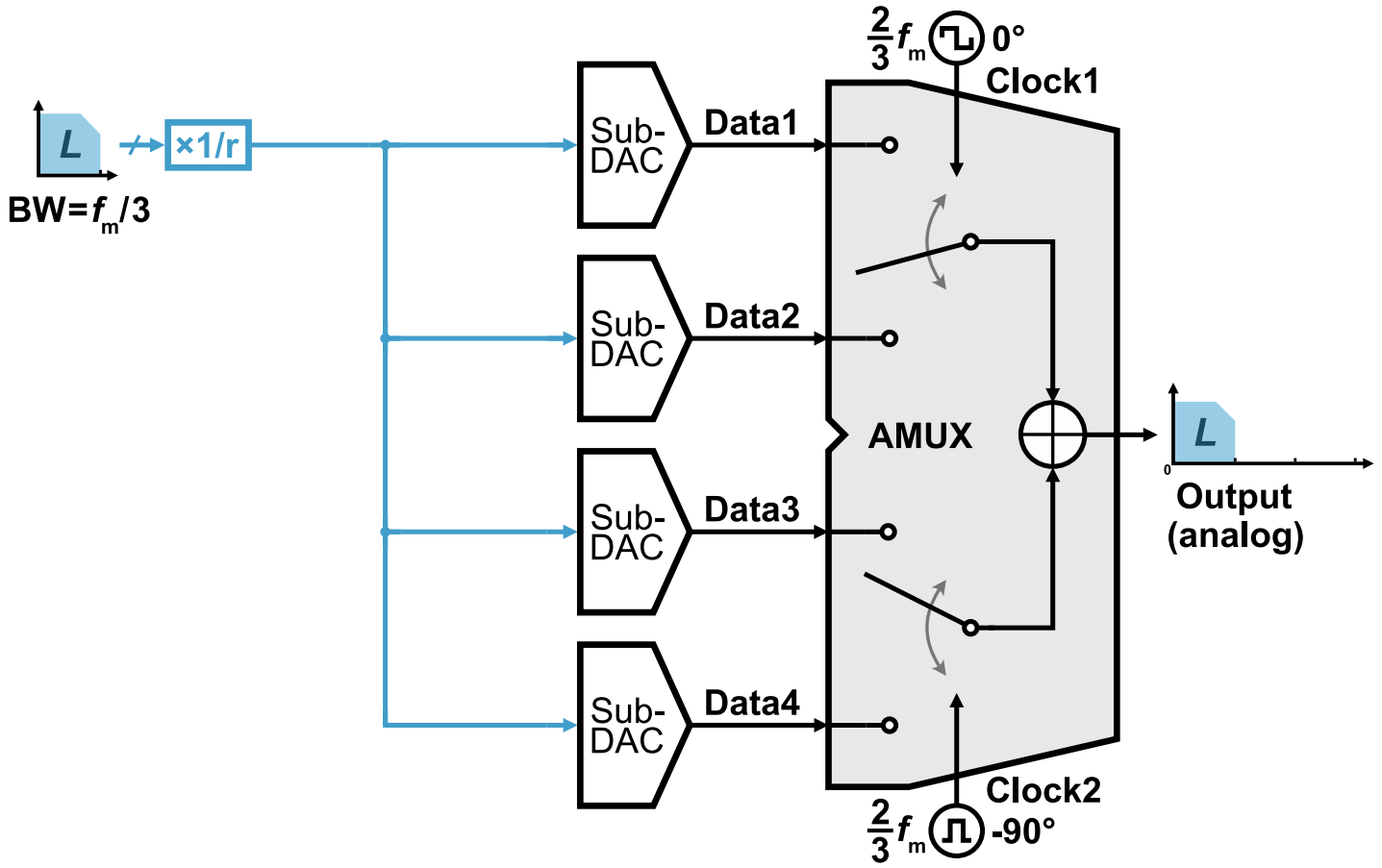
DAC bandwidth tripler



- 😄 No analog filters
- 😄 No delay mismatch
- 😄 Triples bandwidth

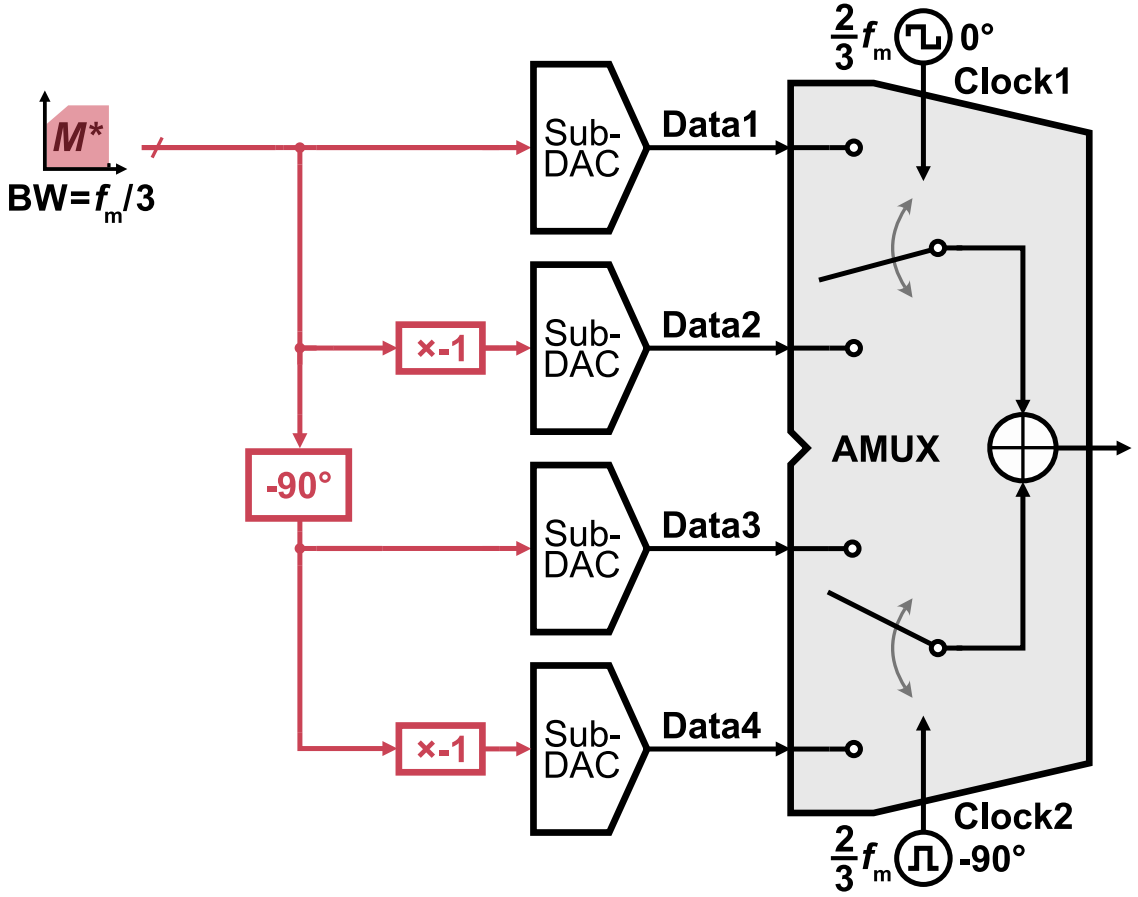
- Our group proposes a “DAC bandwidth tripler”. (Y. Yokoi et al., ICECS 2021)
- Enhances bandwidth by 3 times

Low-band through the AMUX

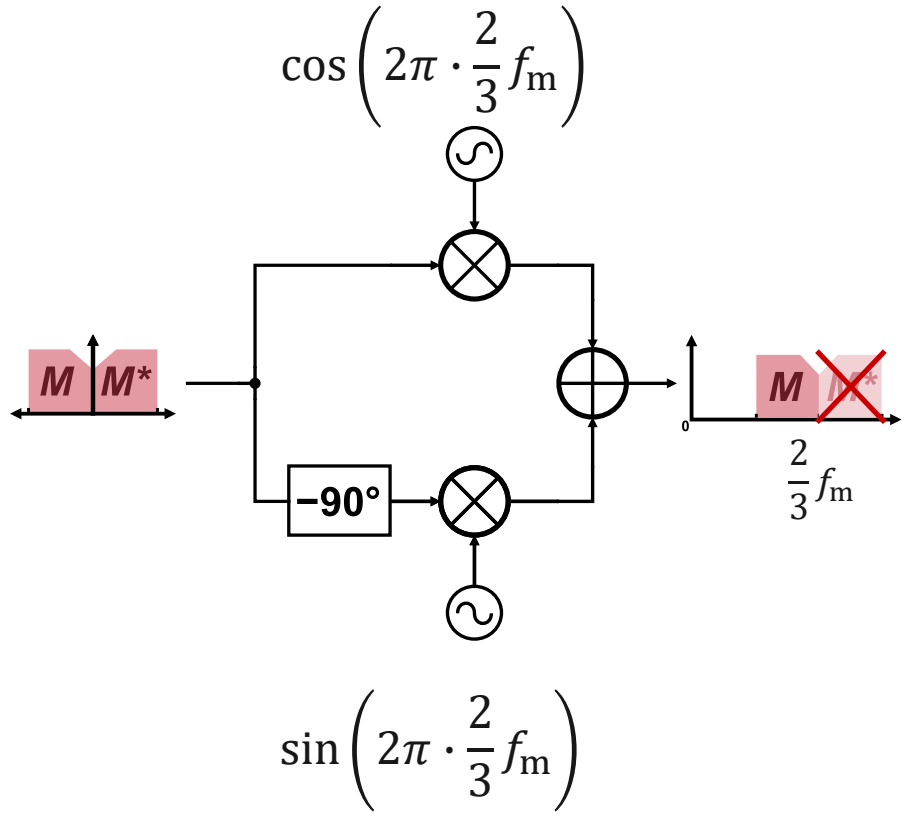


- The same low-band signals are included in all sub-DAC inputs.
- The low-band is output from the AMUX **as it is (i.e., through).**

Mid-band is shifted by 2/3f_m

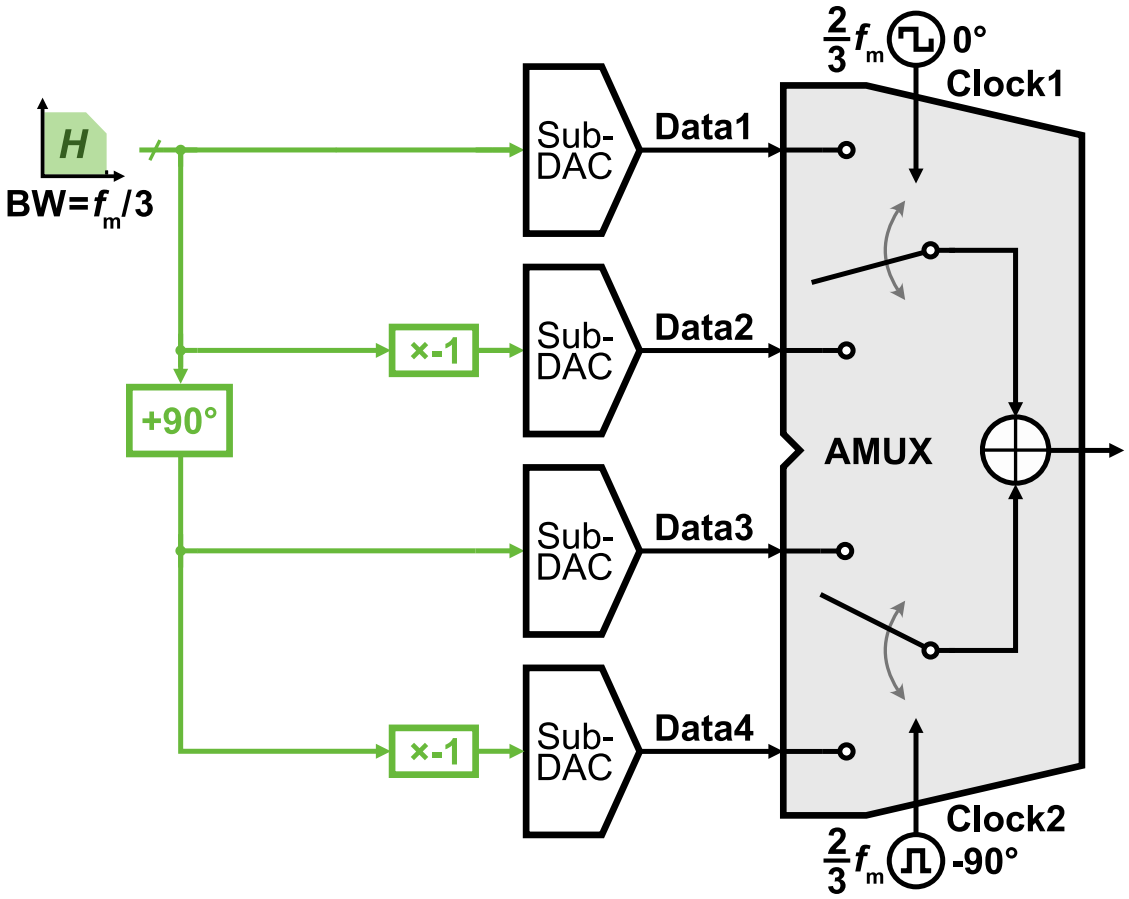


Math. model

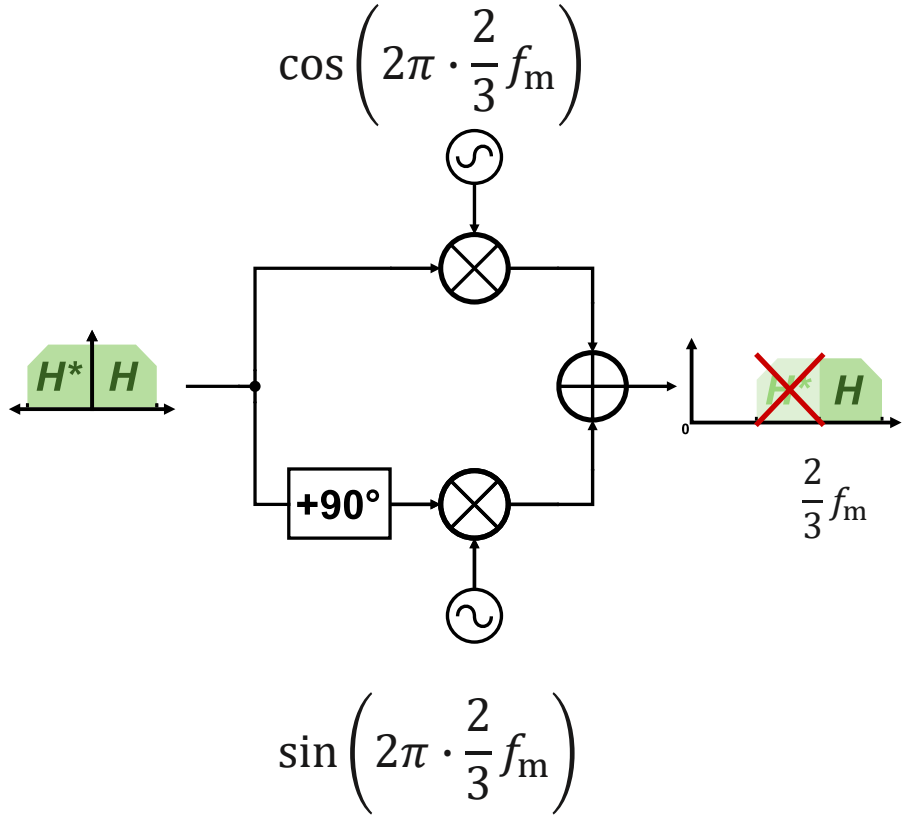


- AMUX operates as a single-sideband (SSB) mixer for the mid-band.
- Only the **lower** sideband is output from the AMUX.

High-band is also shifted by 2/3f_m

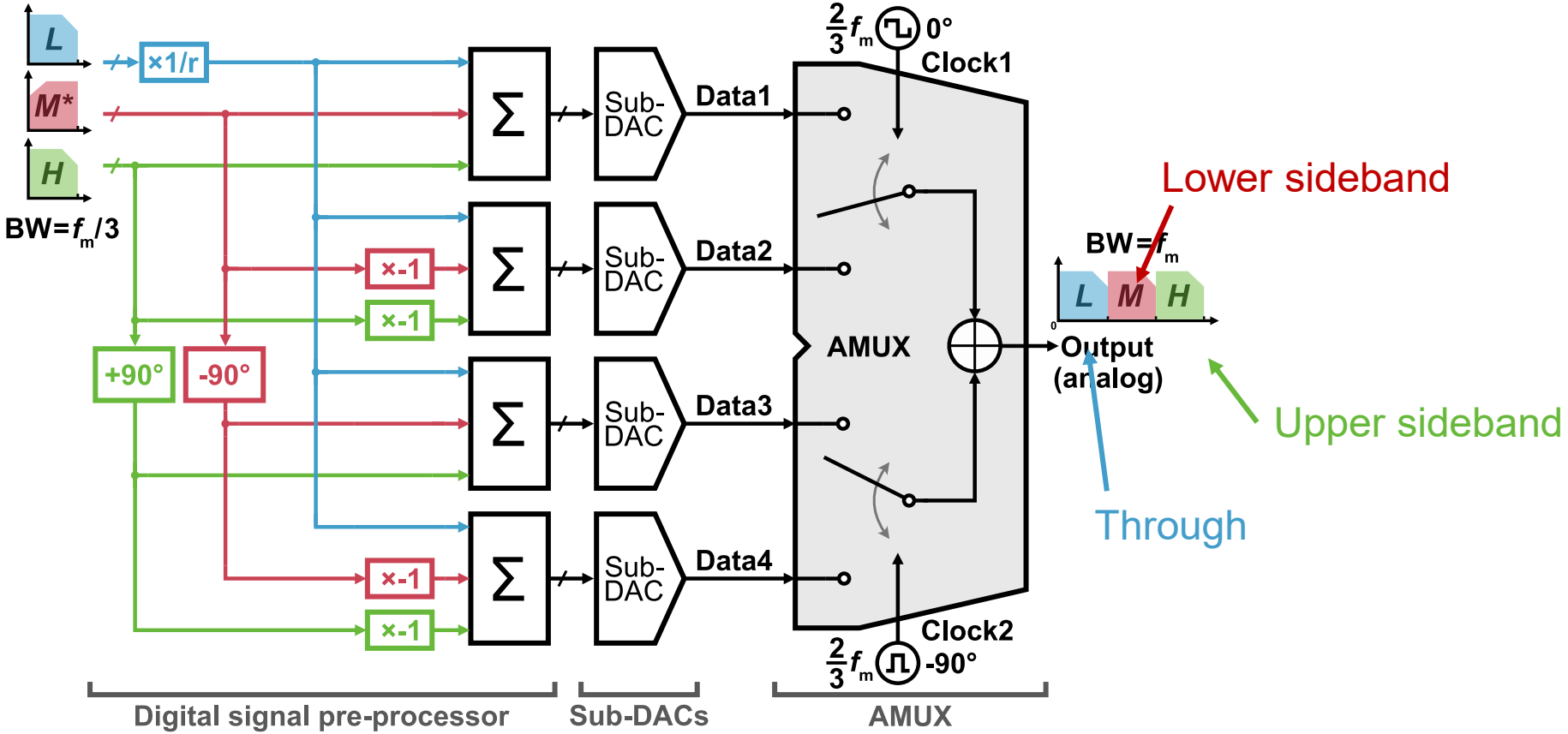


Math. model



- AMUX operates as a single-sideband (SSB) mixer for the high-band.
- Only the **upper** sideband is output from the AMUX.

Whole system again



- Add Low, Mid, and High in advance
- The timing of each sub-band is perfectly aligned.

Challenges

① Development of a **3:1** AMUX-IC

Conventional AMUX-ICs are 2:1 MUX.

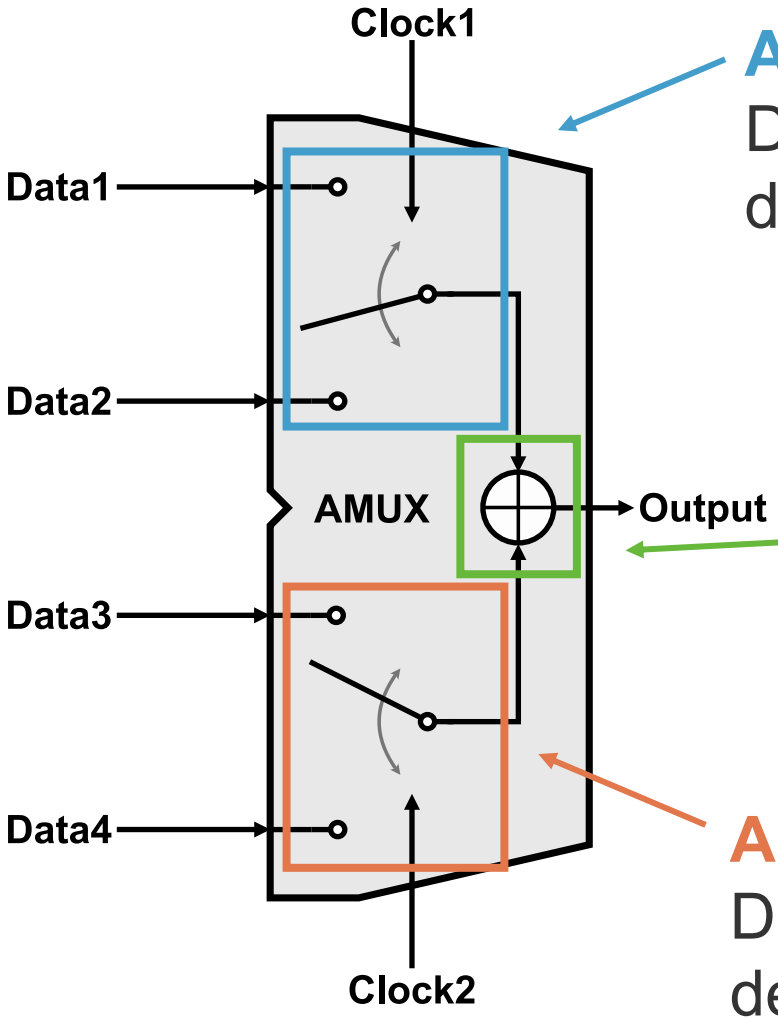
② Reducing power consumption

Conventional AMUX-ICs consume a power of over 500 mW.

To cope with these challenges…

We developed a 3:1 AMUX-IC with a CMOS process in this research.

3:1 AMUX



Alternate switch

Data1 and Data2 are switched depending on the states of ‘High’ or ‘Low’ of Clock1.

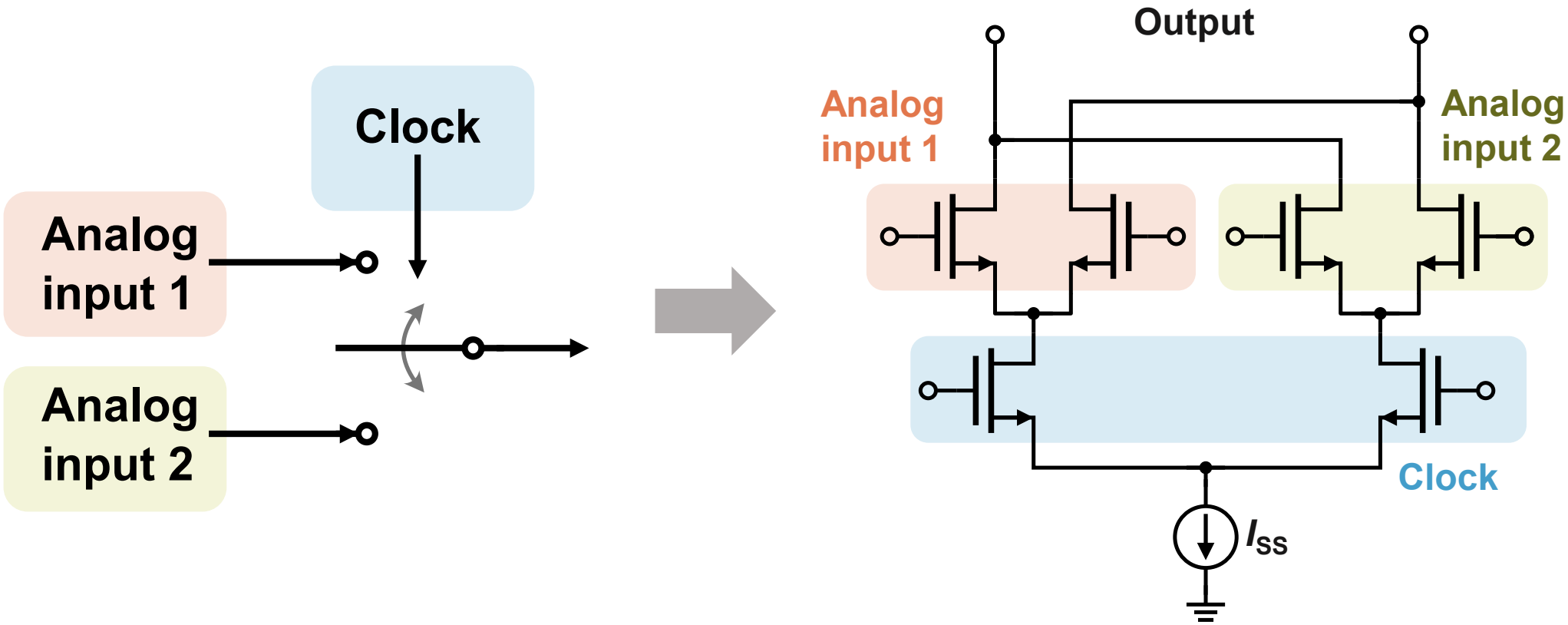
Combiner

The output signals of these switches are added with a combiner.

Alternate switch

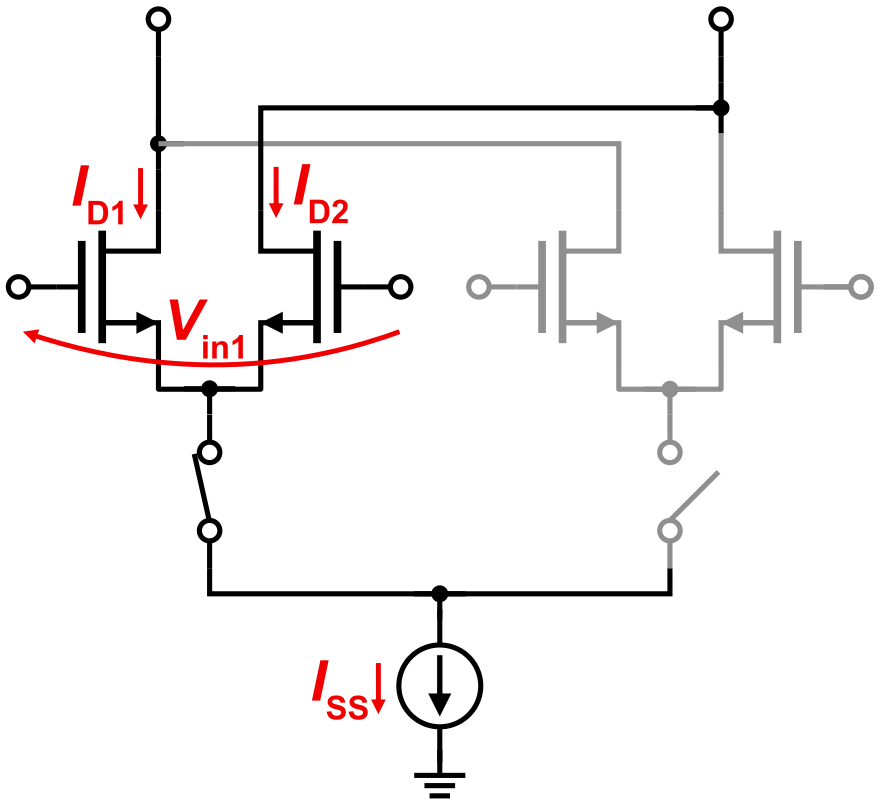
Data3 and Data4 are switched depending on the states of ‘High’ or ‘Low’ of Clock2.

Alternate switch



- Double balanced mixer: ◎High-speed ×Non-linearity
  (Gilbert cell)

Analysis of non-linearity



※β: Gain coefficient of the MOSFET

$$I_{D1} - I_{D2}$$

$$\approx \underbrace{\sqrt{\beta I_{SS}} V_{in1}}_{\text{Fundamental}} - \underbrace{\frac{\beta}{8}\sqrt{\frac{\beta}{I_{SS}}} V_{in1}^3}_{\text{3-rd order distortion}}$$

Ration of the fundamental to the 3rd-order distortion

$$\frac{\frac{\beta}{8}\sqrt{\frac{\beta}{I_{SS}}}}{\sqrt{\beta I_{SS}}} = \frac{\beta}{8I_{SS}} \propto \frac{1}{(V_{GS} - V_{th})^2}$$

→Need to increase $(V_{GS} - V_{th})$ to reduce distortion

Overdrive voltage

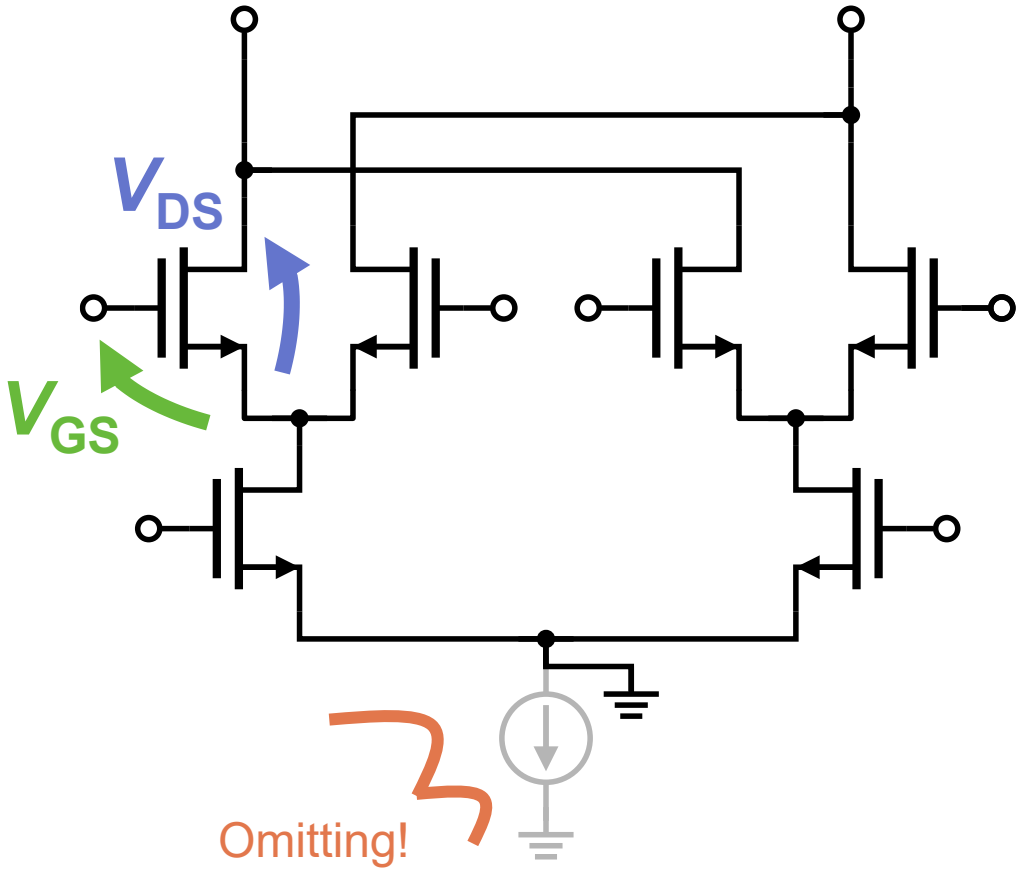
Pseudo-differential switch

For the transistor to operate in the saturation region

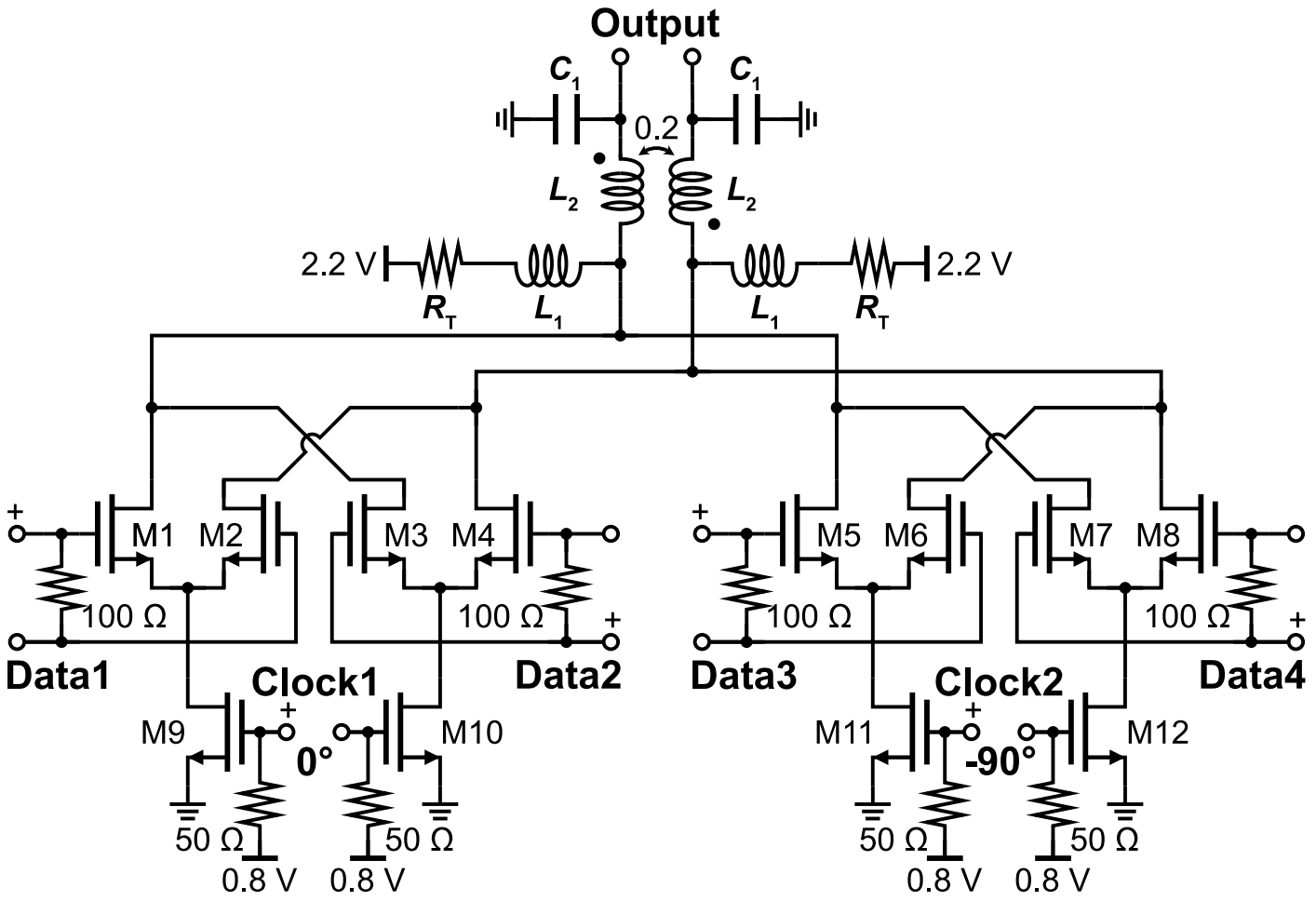
$V_{DS} > V_{GS} - V_{th}$ must be satisfied .

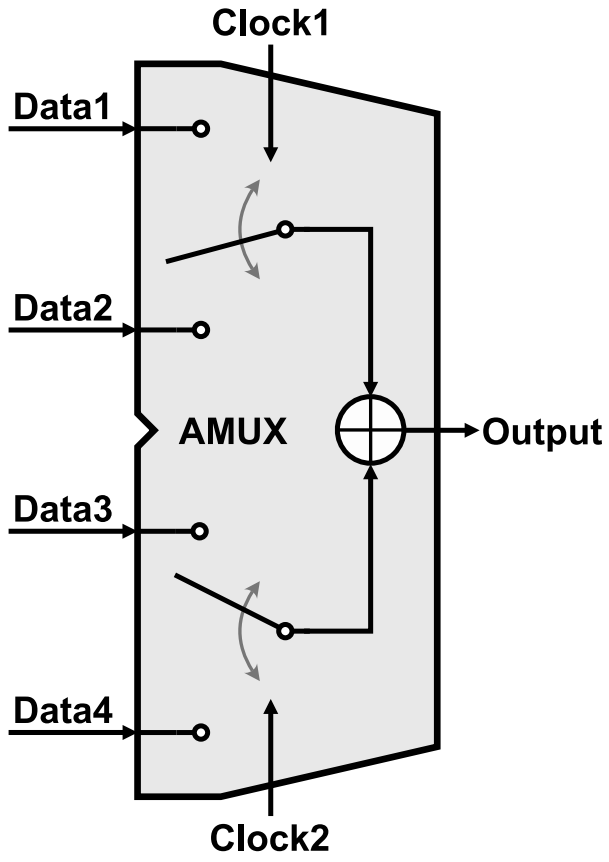
V_{DS} needs to be increased to increase $V_{GS} - V_{th}$

Omitting the current source (Pseudo-differential)

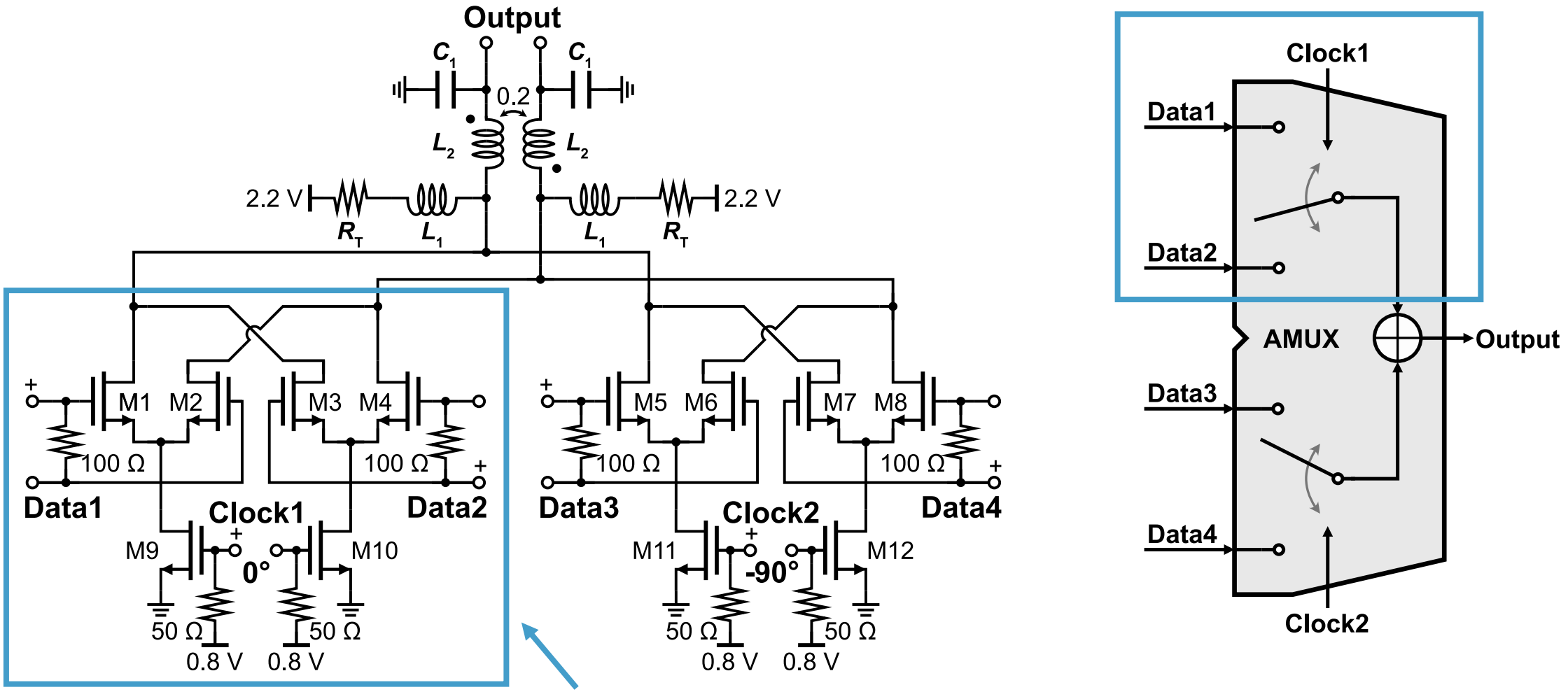


3:1 AMUX (Analog multiplexer)



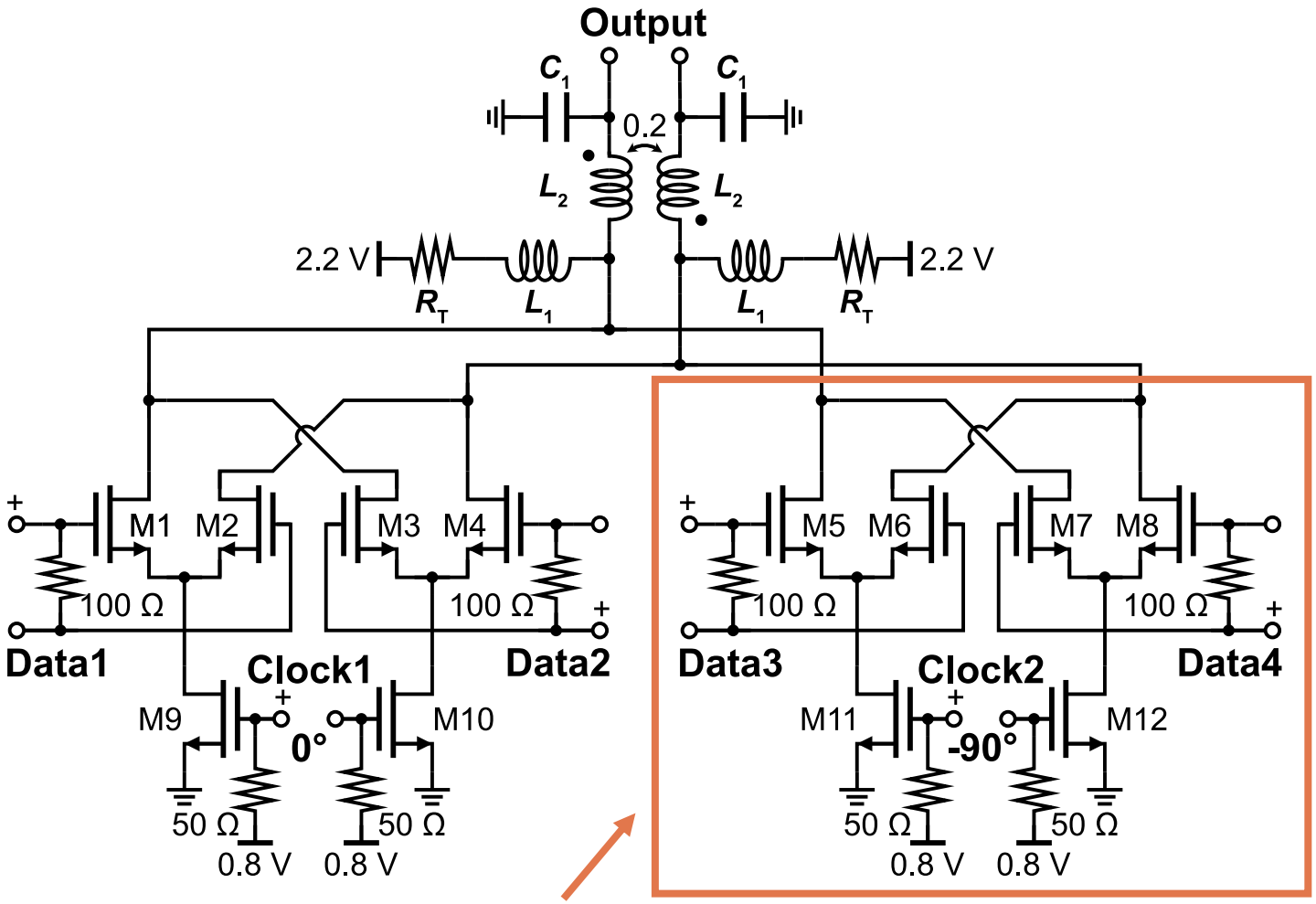


The first switch

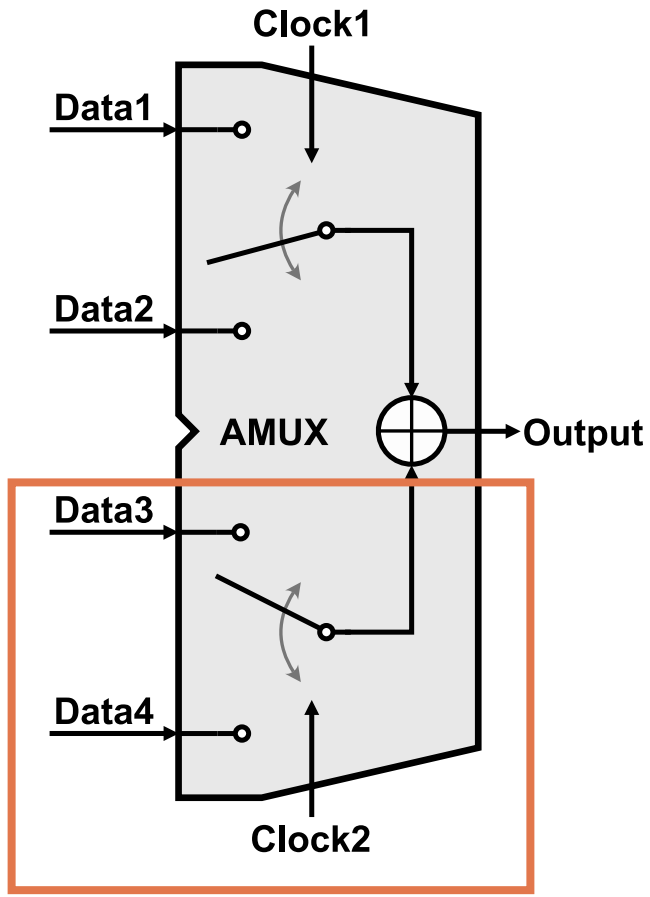


Pseudo differential switch

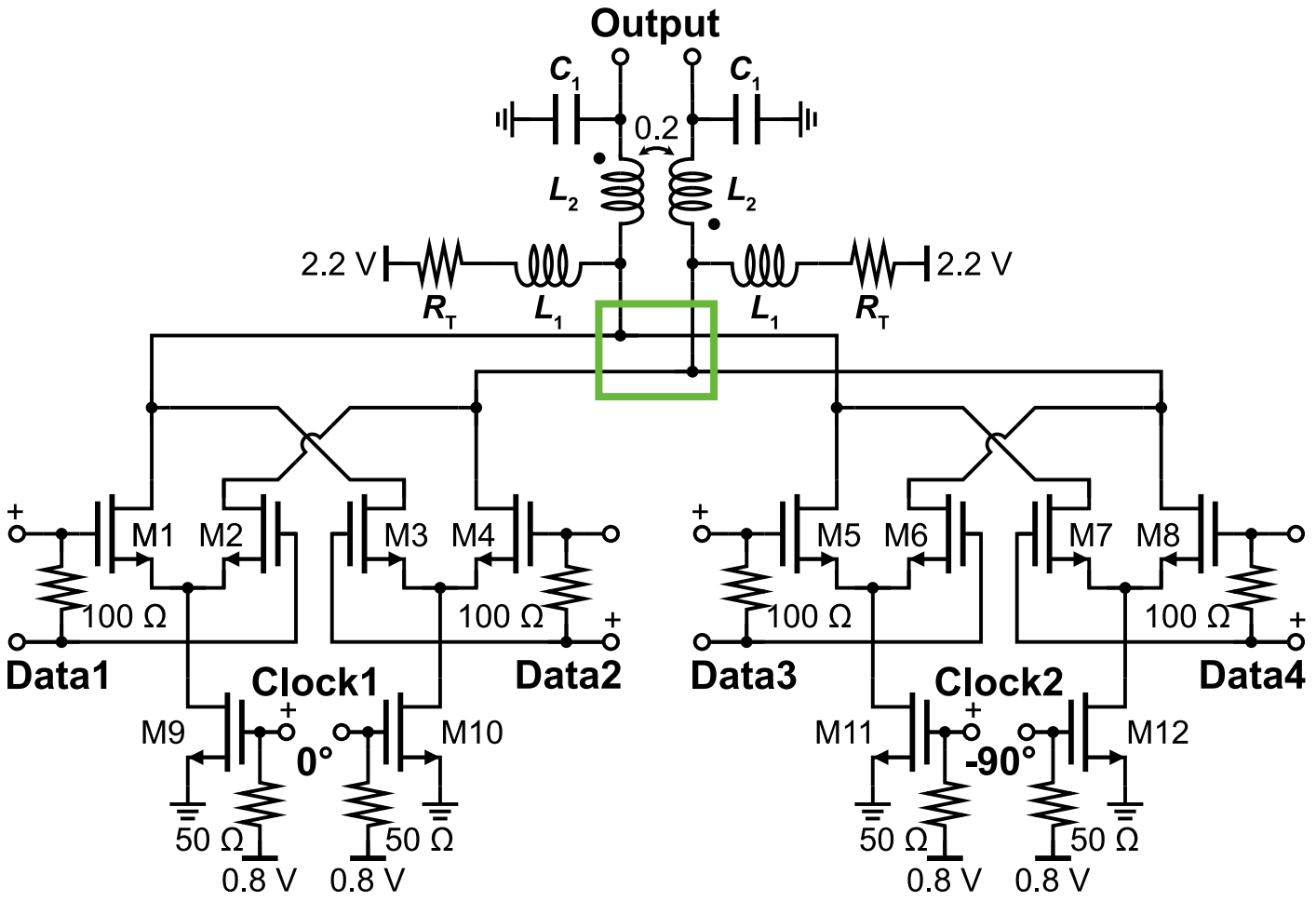
The second switch

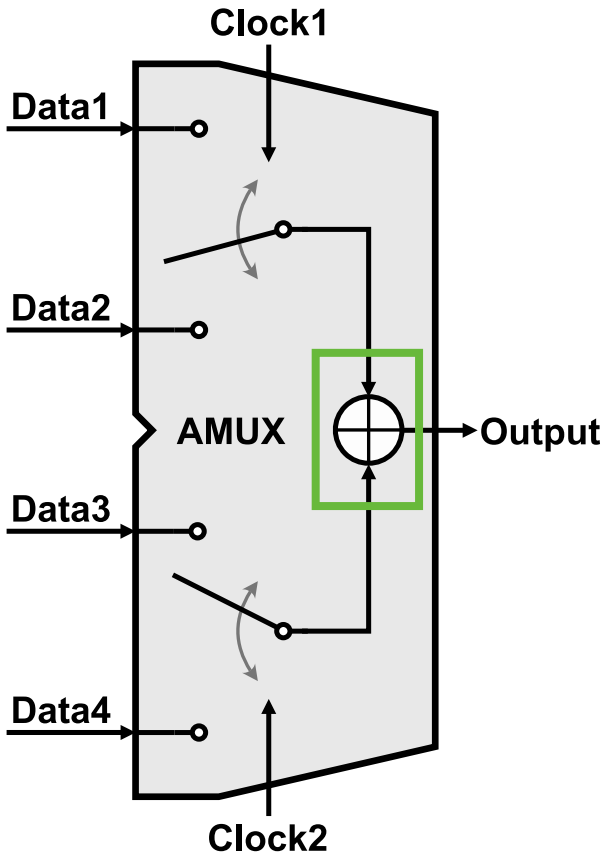


Pseudo differential switch

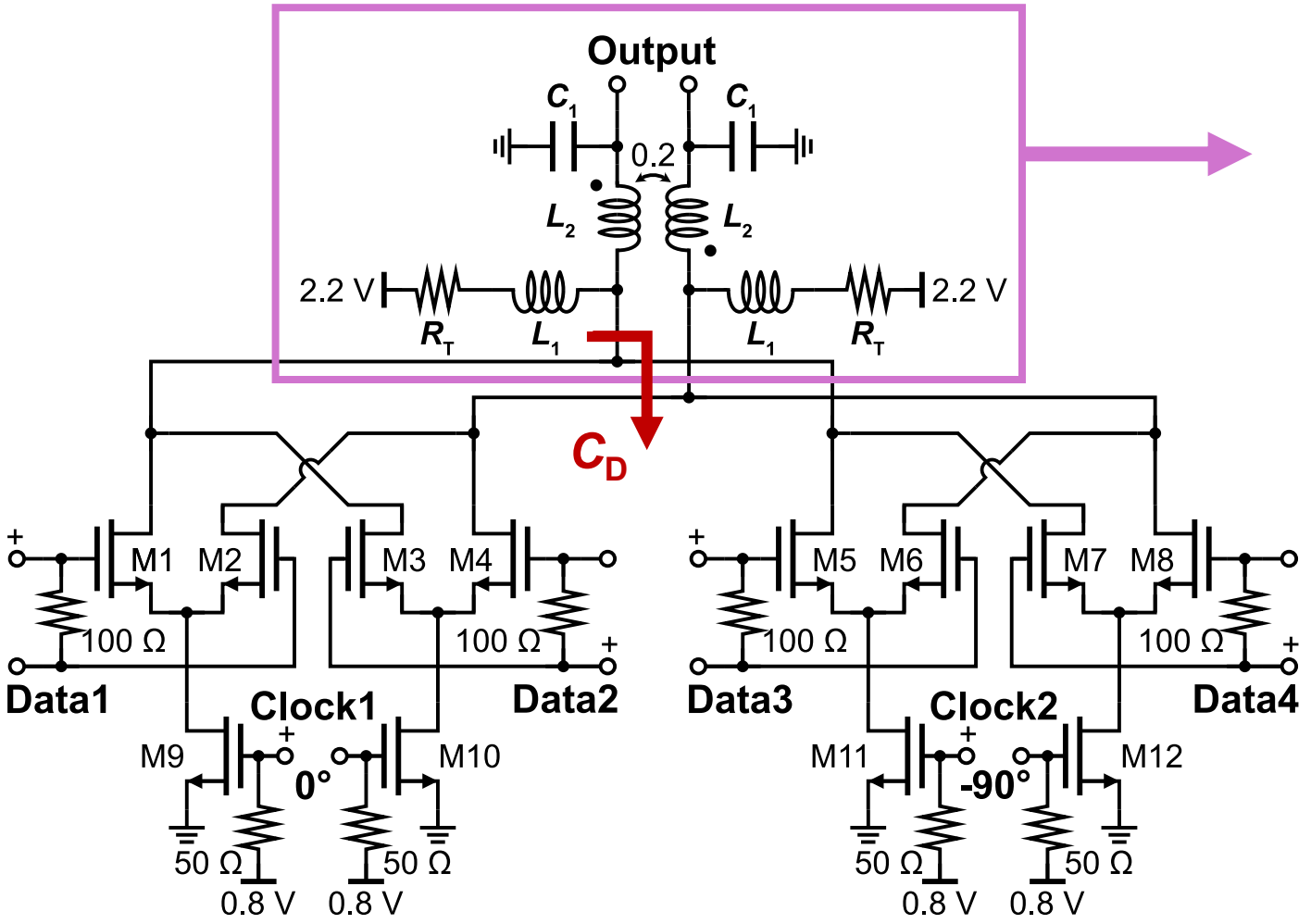


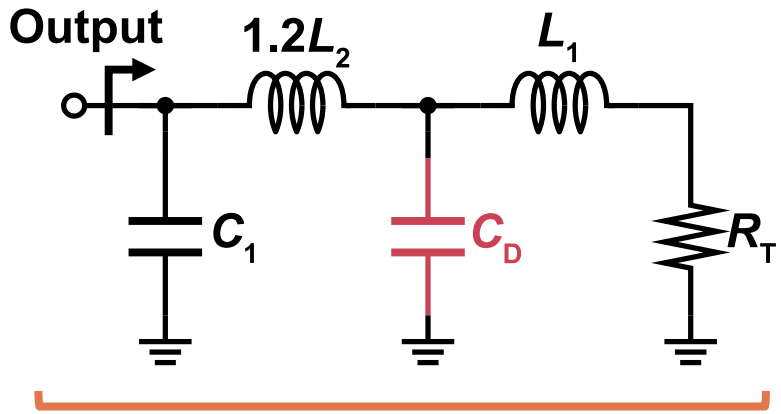
Current mode addition





Broadband termination

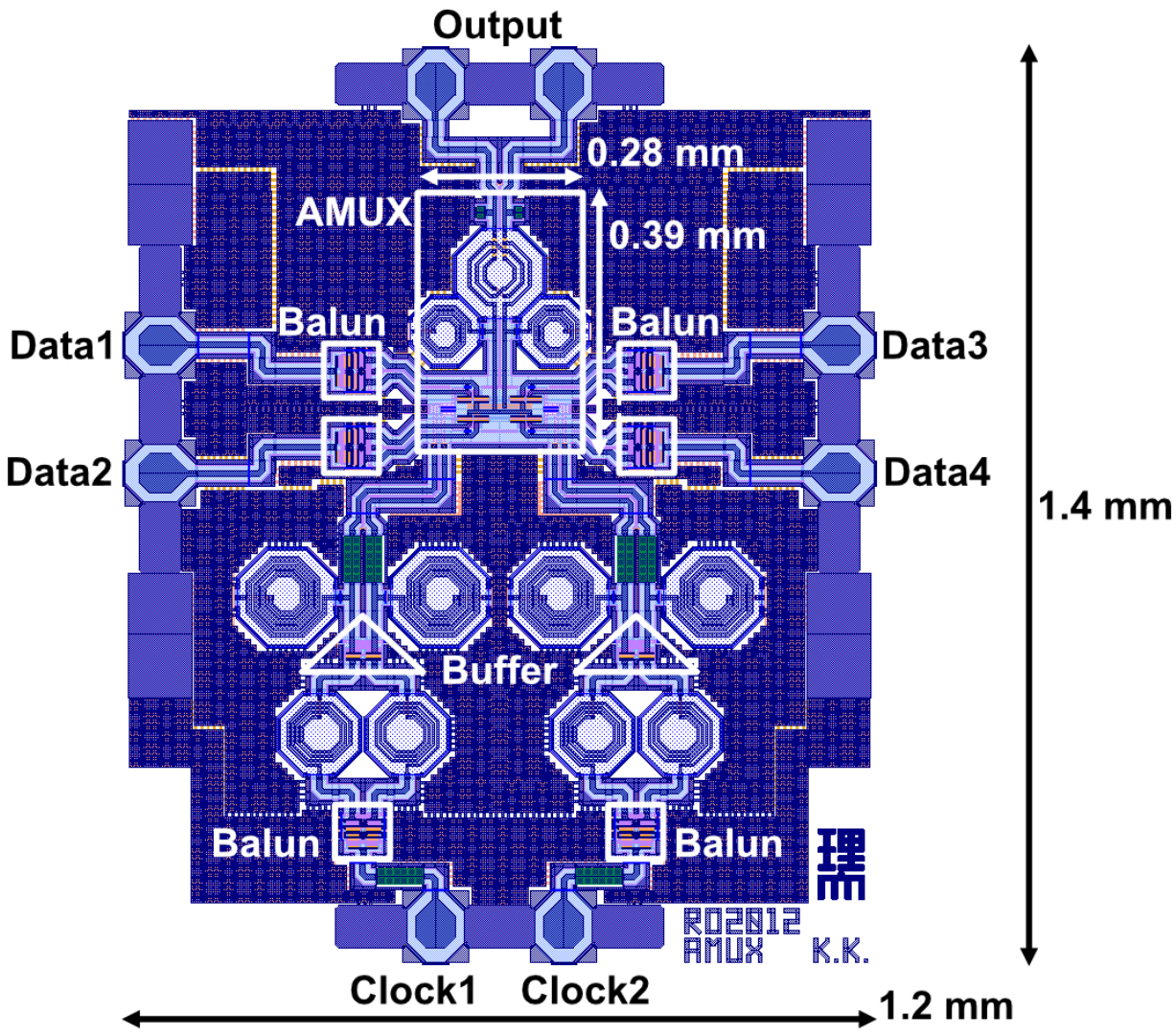




Parasitic capacitor C_D and inductors consist of a **two stage LC ladder**

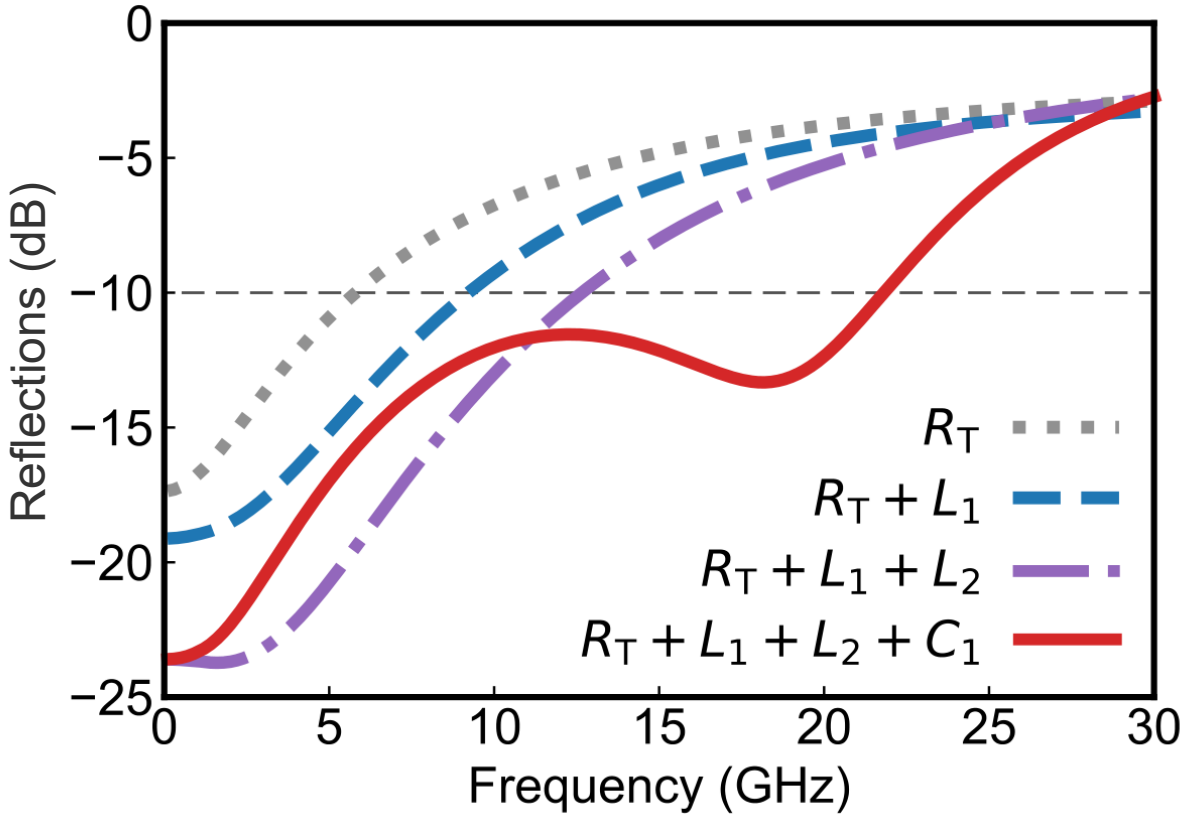
R_T	50 Ω
L_1	450 pH
L_2	300 pH
C_1	130 fF

Layout design



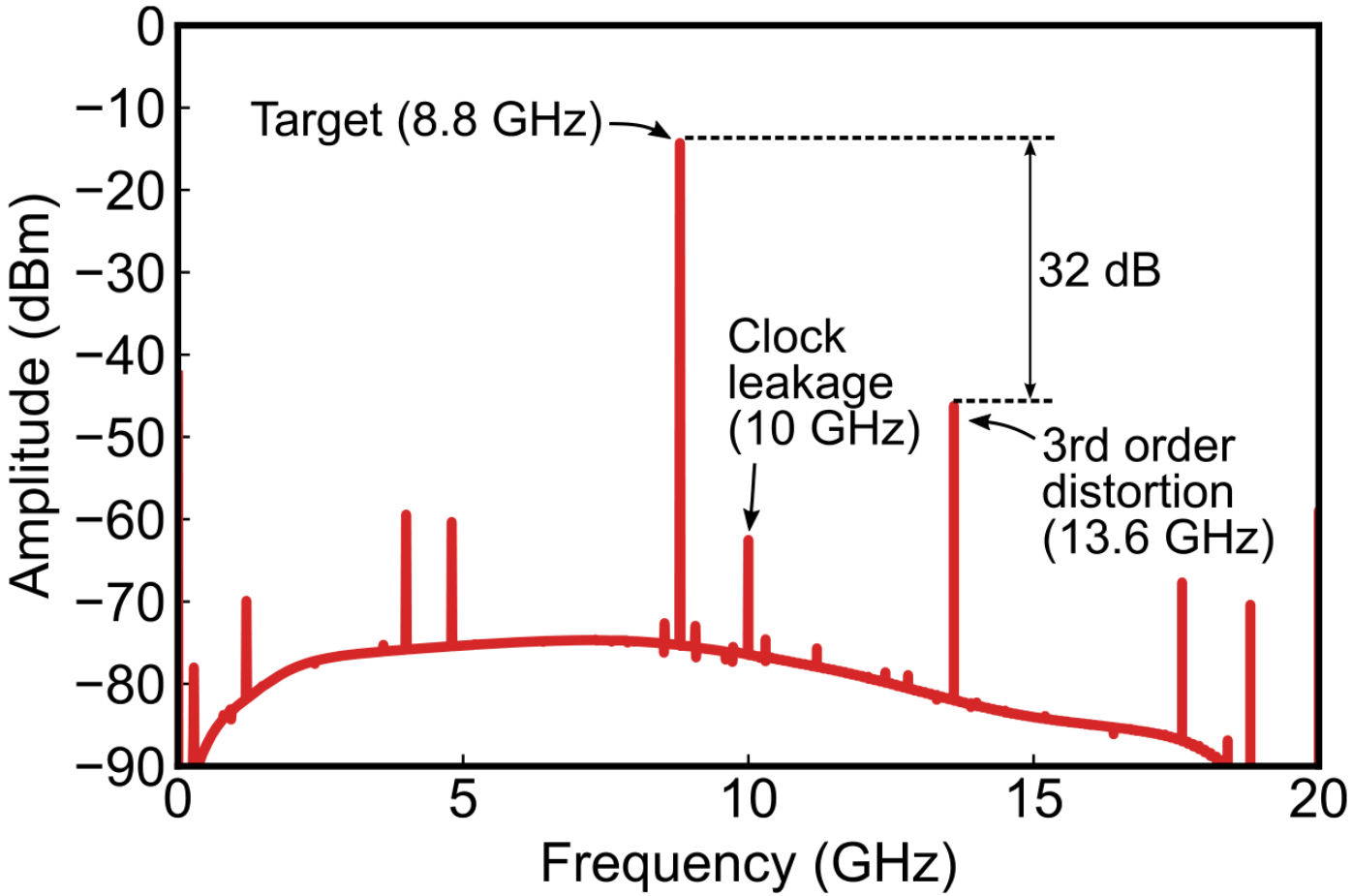
- 180 nm CMOS Technology
- Core area is 0.11 mm^2.
- Baluns are inserted into all inputs to reduce the RF ports.
- Detailed balun design is reported in K. Kawahara et al., MWSCAS 2021.

Output reflections



- Matched bandwidth is 21.4 GHz.
- **3.9x improvement** in matched bandwidth due to L_1 to C_1.

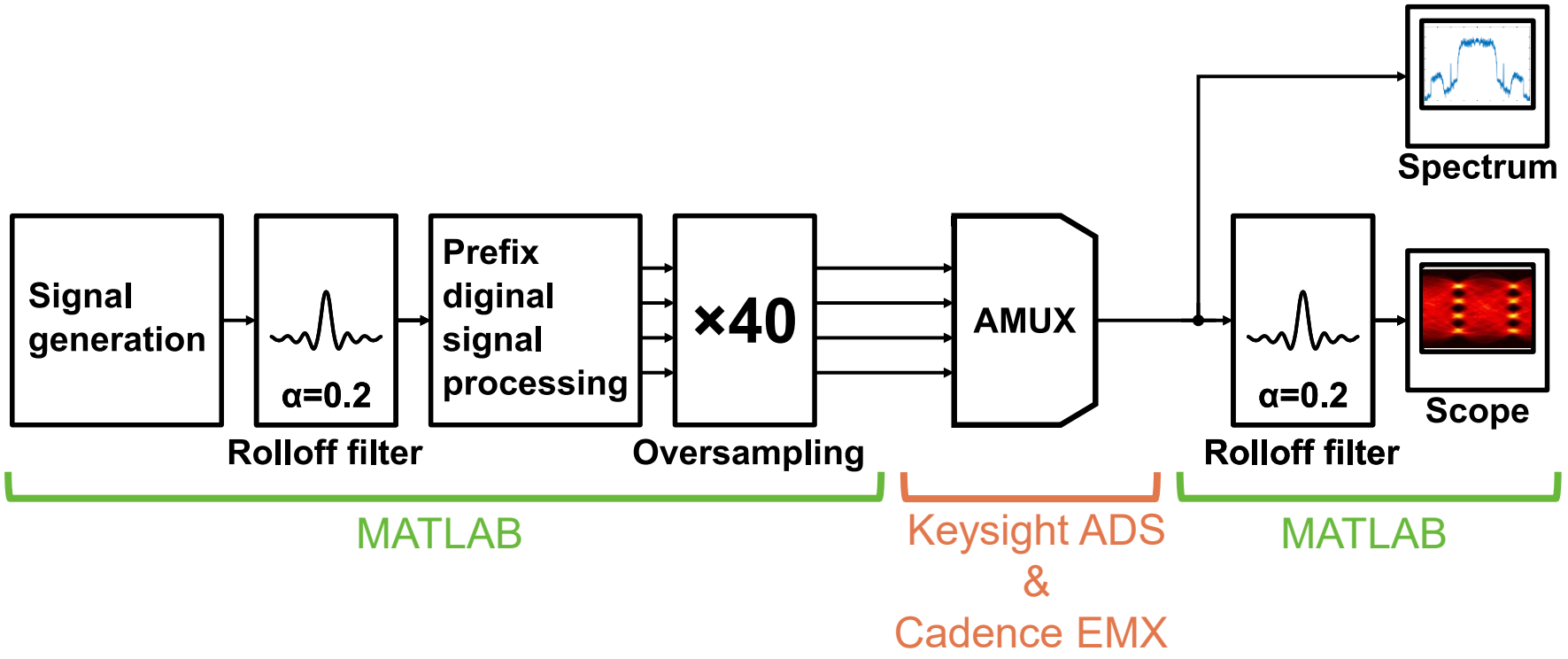
Output spectrum for sine wave



- Data input frequency = 1.2 GHz
- Clock frequency = 10 GHz
- Output lower sideband (8.8 GHz)

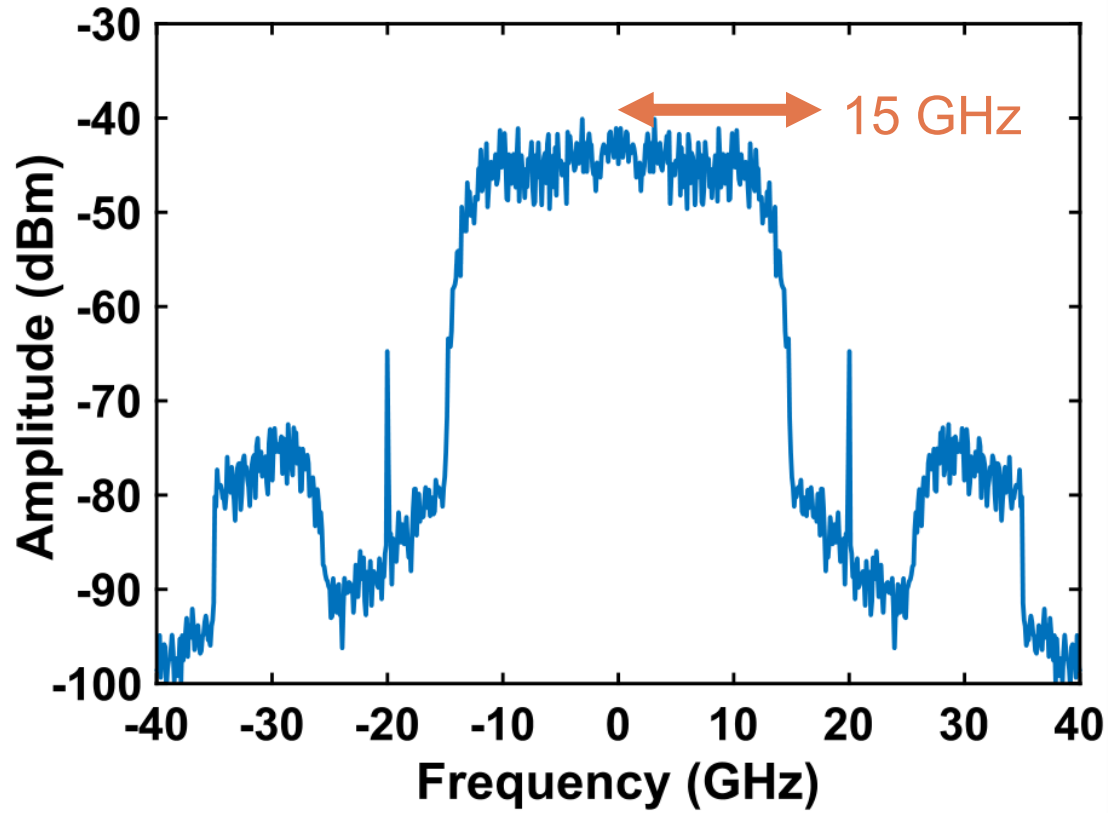
- Satisfy the requirements for PAM4 signal transmission (>30 dB)

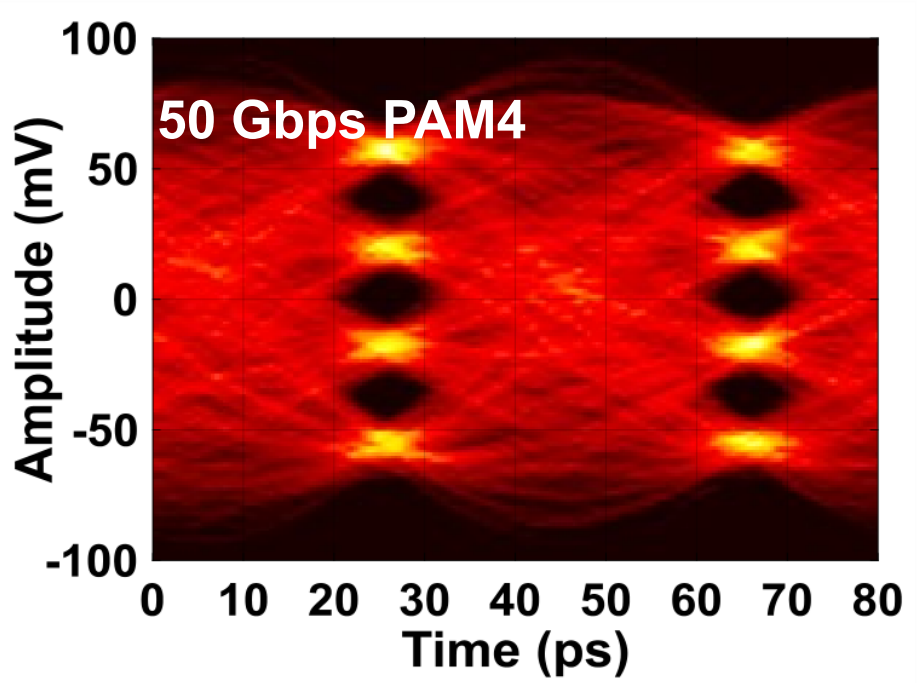
Signal generation test bench



Modulation method	25 Gbaud PAM4
Target bandwidth	15 GHz
Sub-band bandwidth	5 GHz

Signal generation simulation





- Generates a signal with a bandwidth of 15 GHz from an input signal with a bandwidth of 5 GHz
- Power consumption is 49 mW

Comparison with the AMUXes

†Simulation, ‡Excluding the baluns and buffers for measurement

Reference	This work†	[2]	[3]	[4]
Technology	180 nm CMOS	InP HBT	InP HBT	SiGe BiCMOS
fmax (GHz)	65	480	480	500
Multiplication	3:1	2:1	2:1	2:1
Efficiency (pJ/bit)	0.98	4.0	2.9	9.5
−3 dB B.W. (GHz)	22.8	>110	>110	>67
Out. swing (V_{PPD})	0.15	0.5	1.5	0.75
THD (dB)	32	N/A	30	N/A
Baudrate (Gbaud)	25	112	168	56
Baudrate / fmax	0.38	0.23	0.35	0.11
Supply (V)	2.2	-4.5	-4.5	-4.5
Power (mW)	49‡	900	990	1060

- First demonstration of 3:1 AMUX-IC
- Superior power efficiency

Conclusion

- Purposes
  - Realizing high speed digital to analog converters
  - Development of the **3:1** AMUX with **CMOS** process
- Results
  - Low distortion with pseudo differential switches
  - Improved bandwidth with broadband termination
  - 50 Gbps PAM4 signal generation
  - Power efficiency of 0.98 pJ/bit

↪ **Developed techniques improve the bandwidth and power efficiency of optical transmitters !**