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A Broadband Active Balun with Inductor-Less Active Peaking and Imbalance Correction

Keisuke Kawahara, Yohtaro Umeda, and Kyoya Takano

Department of Electrical Engineering, Graduate School of Science and Technology, Tokyo University of Science

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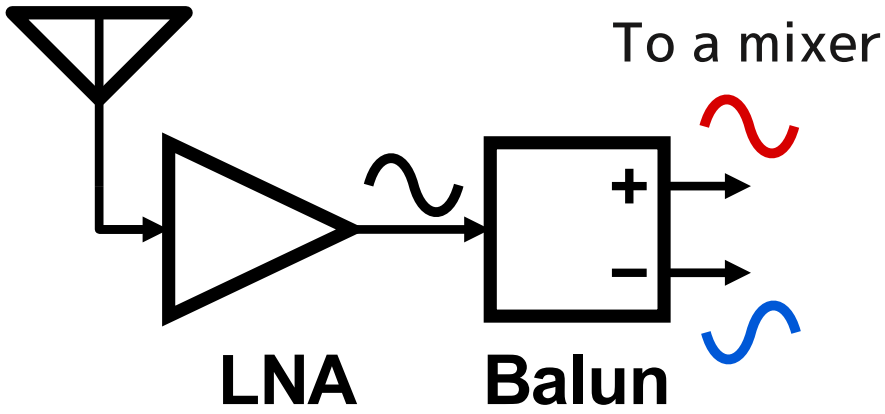
Outline

1. Background
2. Analysis and design
   A) Magnitude and Phase Concurrent Correction Technique
   B) Active Peaking Technique
   C) Design Example
3. Simulation and Results
   A) Pre-layout Simulation
   B) Post-layout Simulation
4. Conclusion

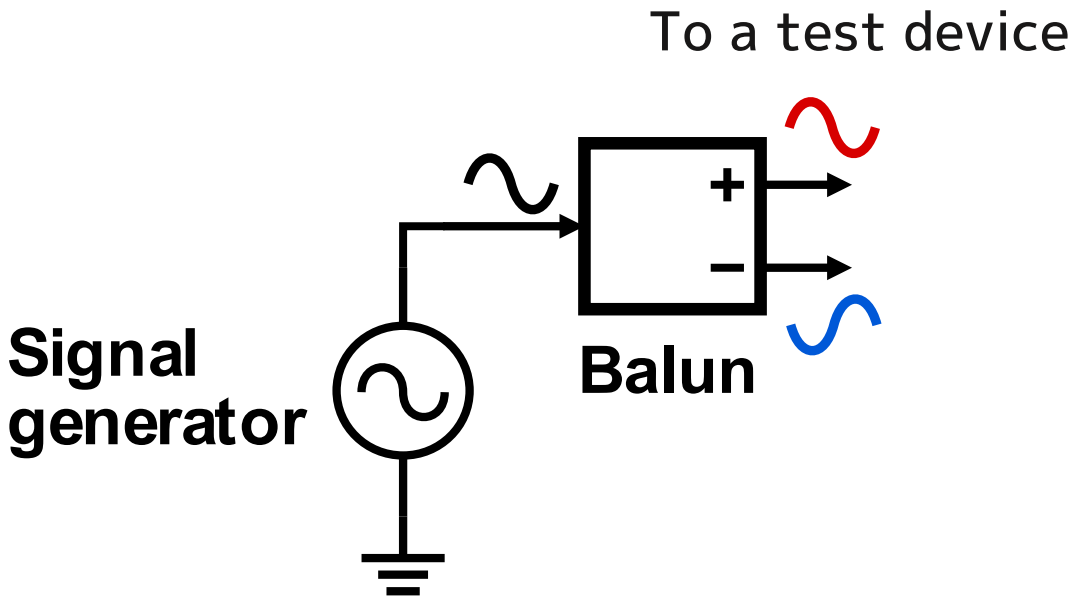
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Microwave baluns



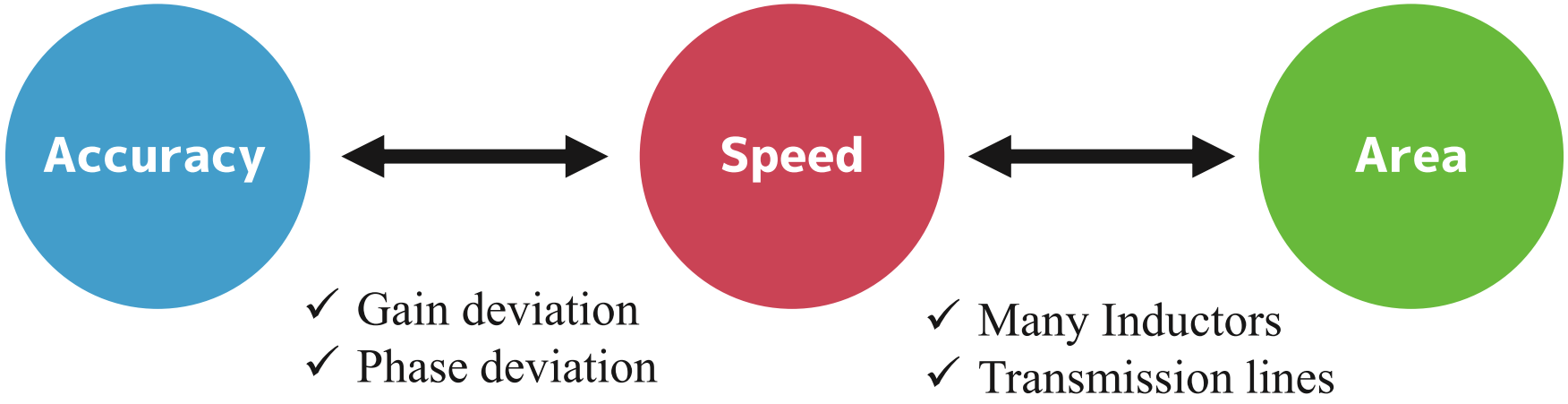
Wireless receivers



Experiment or measurement

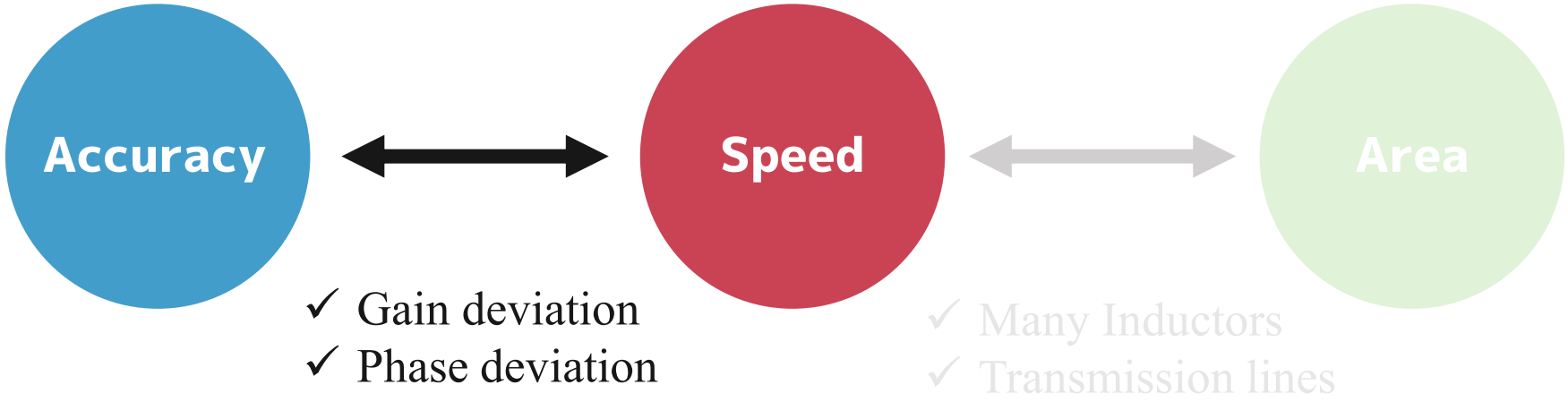
- Baluns are used for single-ended/differential conversion

Balun trade-offs



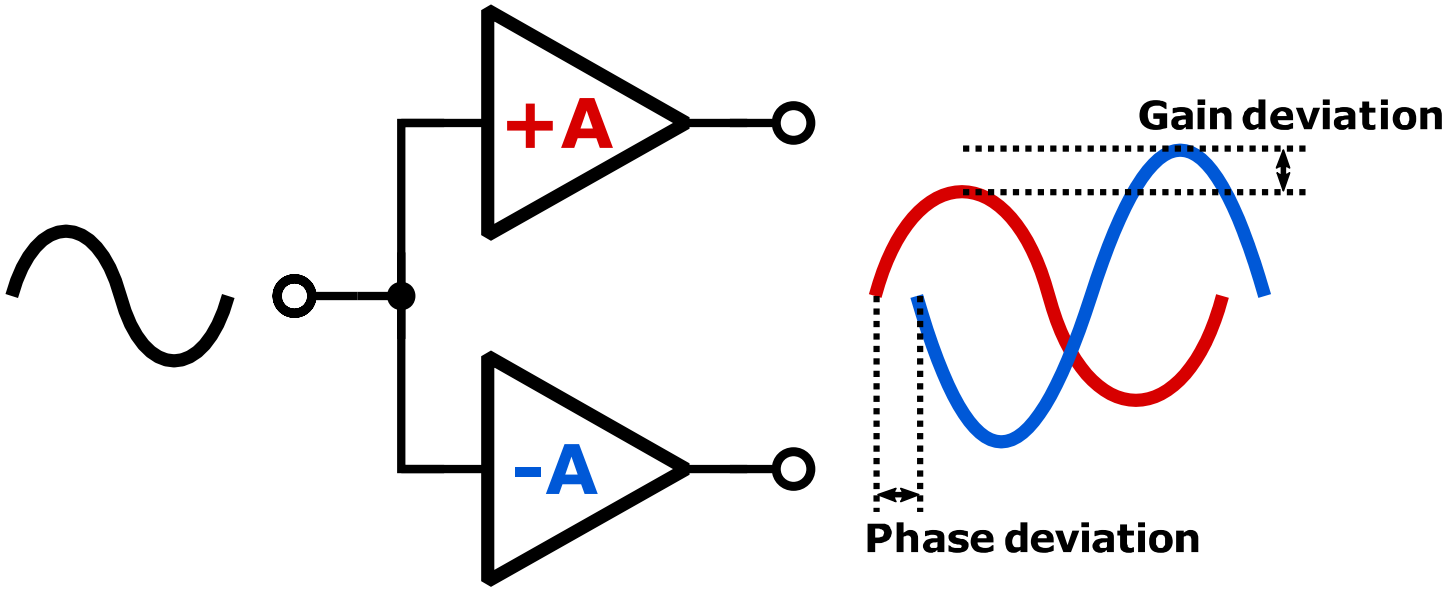
1. Gain and phase deviations increase at high frequencies
2. Inductors or transmission lines (T-lines) increase chip-areas

Balun trade-offs



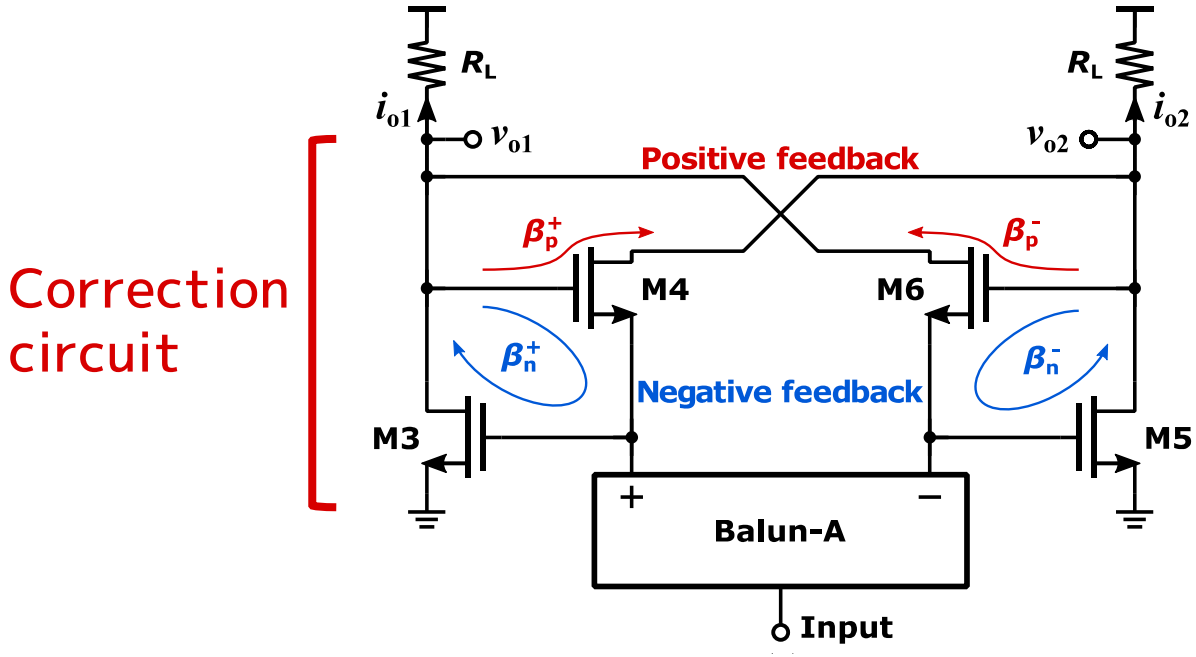
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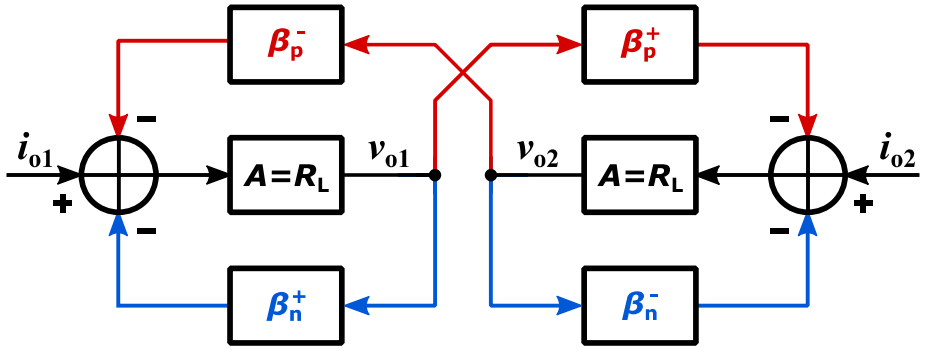
Gain and phase deviations



- Gain and phase deviations increase at high frequencies
  - Due to the large immittance of parasitic elements
  - Due to process variations

MPCCT (Magnitude and Phase Concurrent Correction Technique[1])

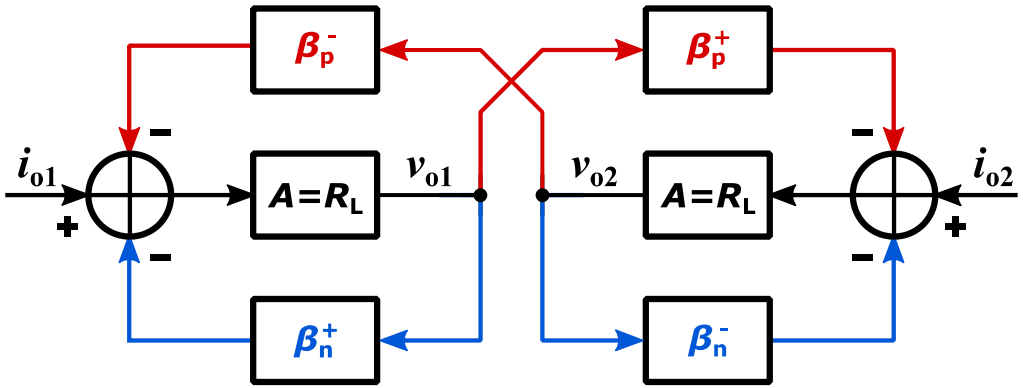




Block diagram of the correction circuit

- Correction circuit reduces the deviations

MPCCT (Magnitude and Phase Concurrent Correction Technique[1])



$$\boldsymbol{v_{o1}} = \frac{1}{\delta}\left[\left(\frac{1}{A} + \beta_n^-\right)\boldsymbol{i_{o1}} - \beta_p^-\boldsymbol{i_{o2}}\right] \quad (1)$$

$$\boldsymbol{v_{o2}} = -\frac{1}{\delta}\left[\beta_p^+\boldsymbol{i_{o1}} - \left(\frac{1}{A} + \beta_n^+\right)\boldsymbol{i_{o2}}\right] \quad (2)$$

※ δ is a constant coefficient

- When $\left(\frac{1}{A} + \beta_n\right) = \beta_p$, deviations are perfectly corrected
  - but the loop gain of the positive feedback becomes one, which causes a stability problem😫
- This work clarifies the relation between CMRR and stability!

CMRR of the MPCCT

- From eq. (1) and (2)

$$\boldsymbol{v_{com}} = \frac{\boldsymbol{v_{o1}} + \boldsymbol{v_{o2}}}{2} = \frac{1}{\delta} \cdot \frac{\left(\frac{1}{A} + \beta_n^- - \beta_p^+\right)\boldsymbol{i_{o1}} + \left(\frac{1}{A} + \beta_n^+ - \beta_p^-\right)\boldsymbol{i_{o2}}}{2}, \tag{3}$$

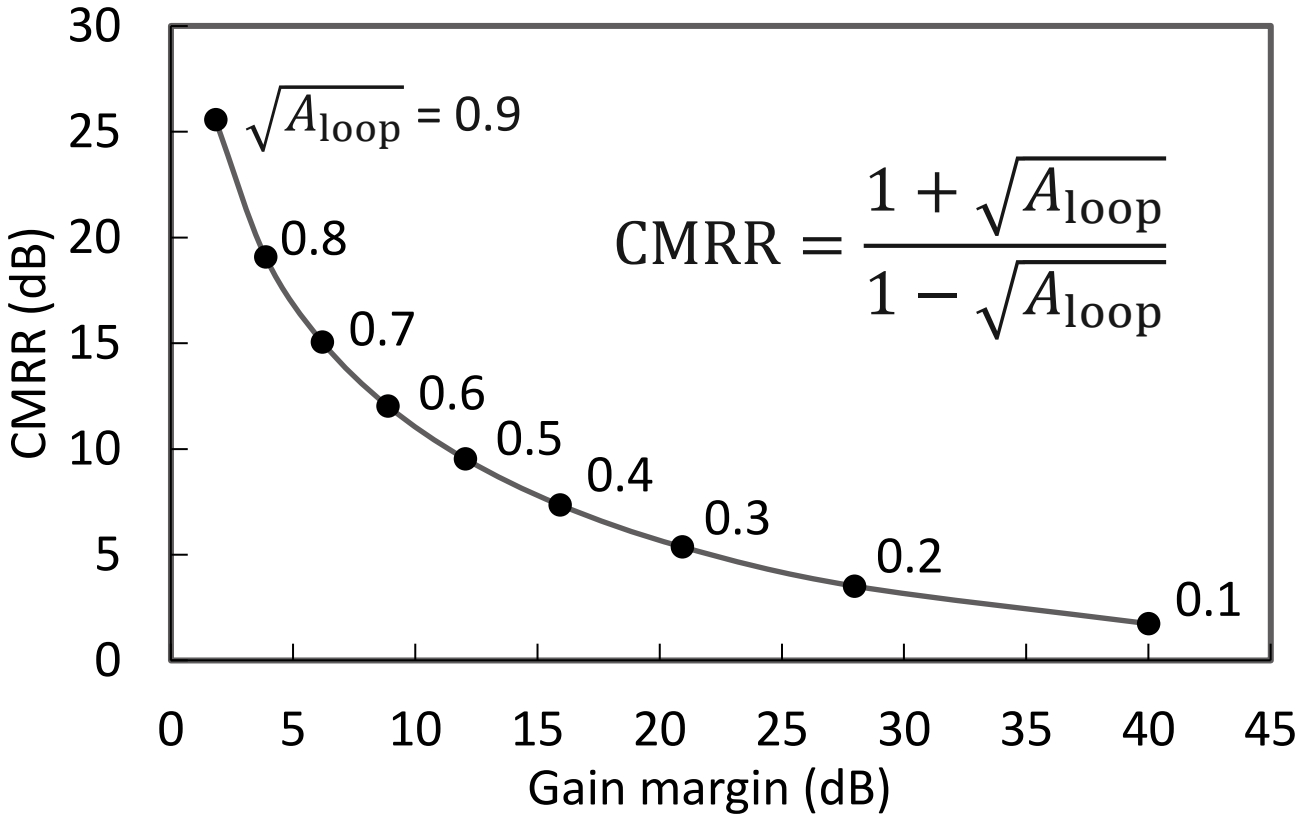
$$\boldsymbol{v_{dif}} = \frac{\boldsymbol{v_{o1}} - \boldsymbol{v_{o2}}}{2} = \frac{1}{\delta} \cdot \frac{\left(\frac{1}{A} + \beta_n^- + \beta_p^+\right)\boldsymbol{i_{o1}} - \left(\frac{1}{A} + \beta_n^+ + \beta_p^-\right)\boldsymbol{i_{o2}}}{2}. \tag{4}$$

→ MPCCT makes v_{com} smaller compared with v_{dif}.

- $$\mathrm{CMRR} = \frac{\frac{1}{A} + \beta_n + \beta_p}{\frac{1}{A} + \beta_n - \beta_p} = \frac{1 + \sqrt{A_{loop}}}{1 - \sqrt{A_{loop}}},$$

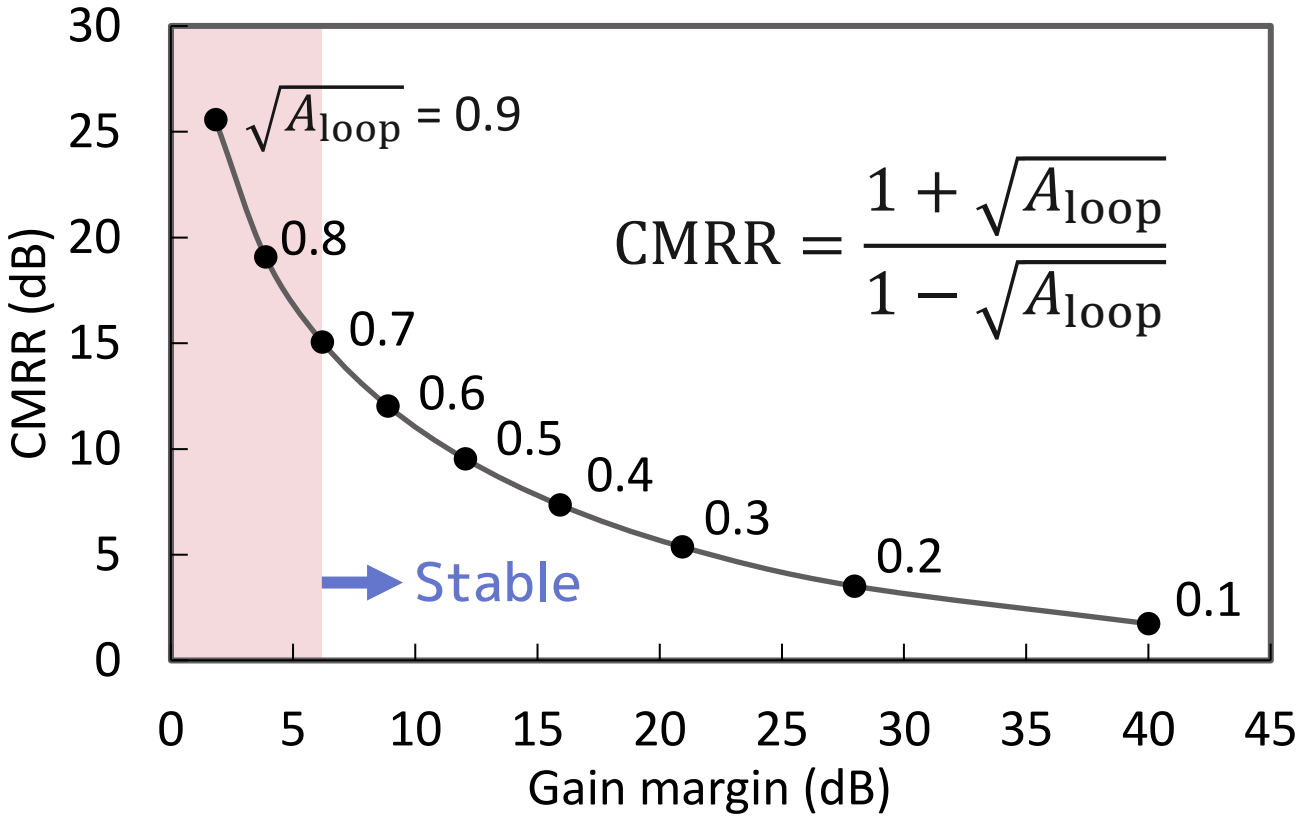
$A_{loop} \equiv \left(\frac{A\beta_p}{1+A\beta_n}\right)^2$ is the loop gain of the positive feedback

CMRR vs. Gain margin



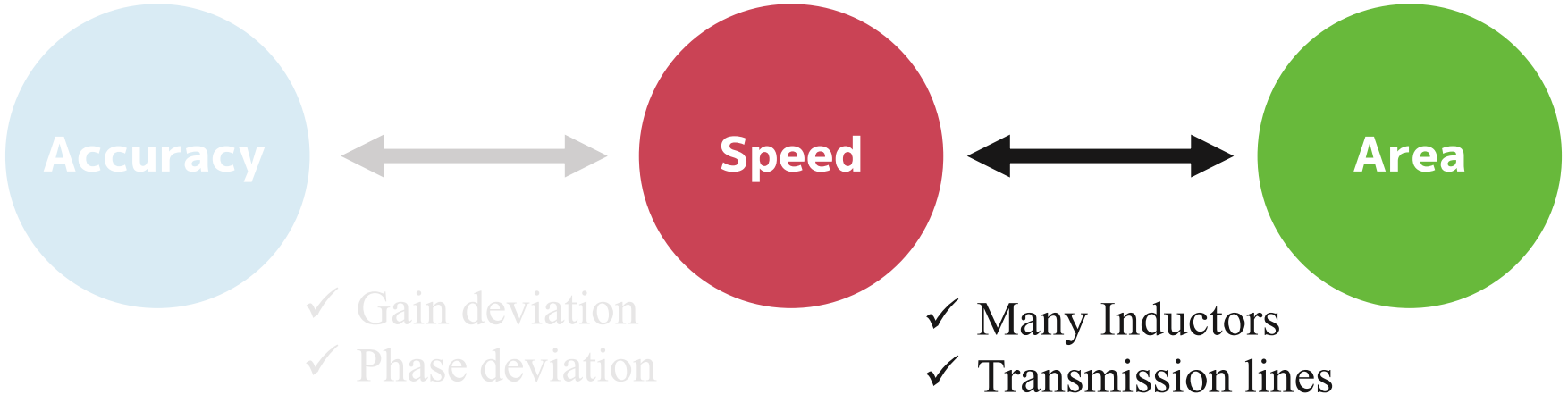
- Reducing the gain margin improves the CMRR

CMRR vs. Gain margin



- The CMRR is limited up to 15 dB for stability in practice

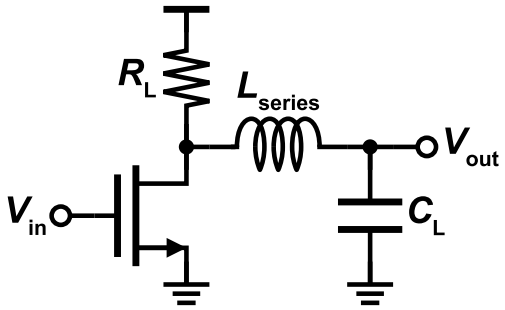
Balun trade-offs



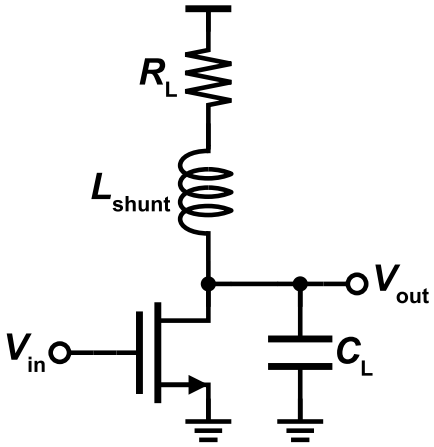
1. Gain and phase deviations increase at high frequencies
2. Inductors or transmission lines (T-lines) increase chip-areas

Inductive peaking

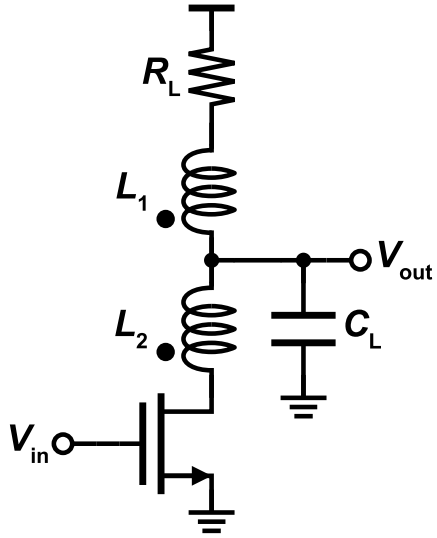
Series peaking



Shunt peaking



T-coil peaking

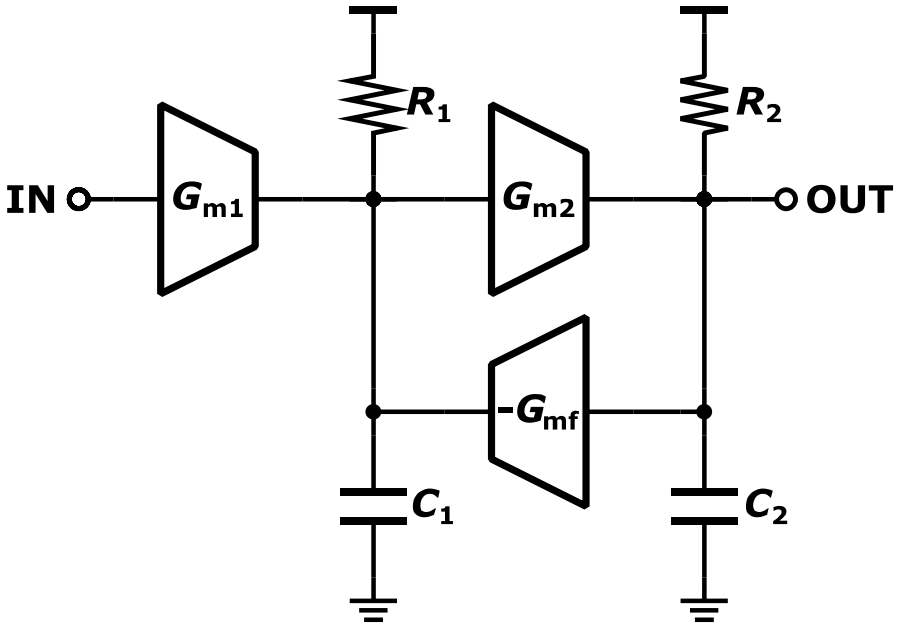


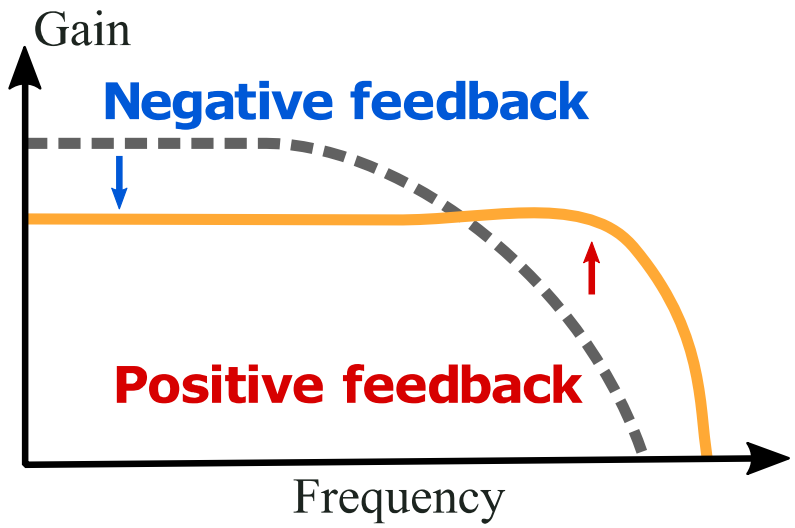
GBWs ×1.41 ×1.83 ×2.85

- Inductor or T-lines are used for bandwidth enhancement
- Inductive components occupy large chip-area

Active peaking technique (APT)

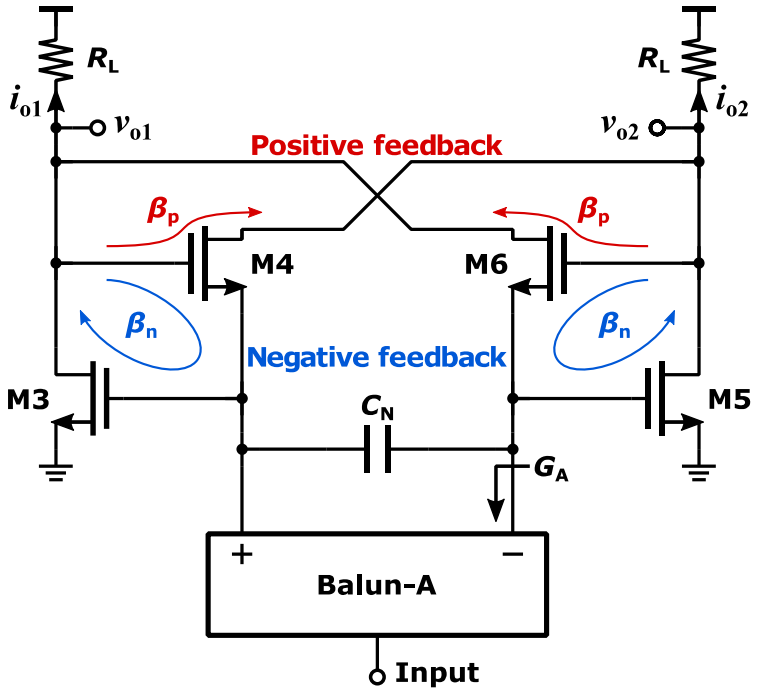
S. Galal et al., J.SSC, 38(12), 2003.

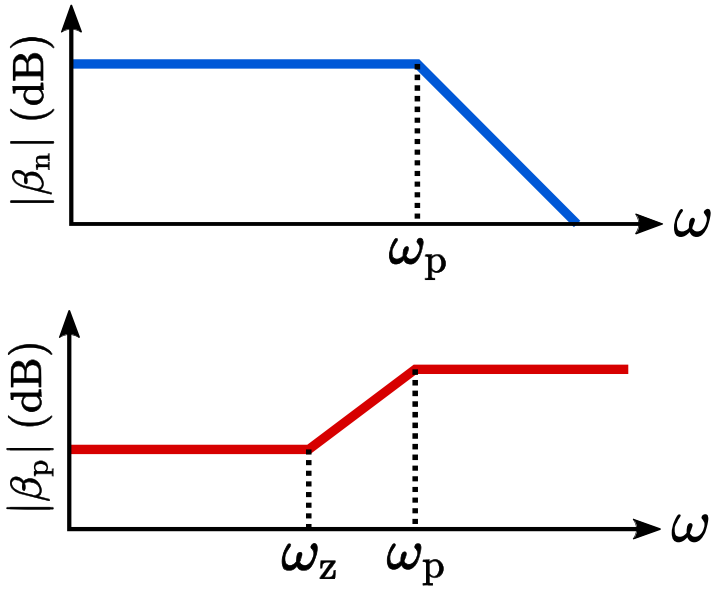




- Low freq. → No phase delay → Negative feedback
- High freq. → C_1 and C_2 delay the phase → Positive feedback

Proposed APT



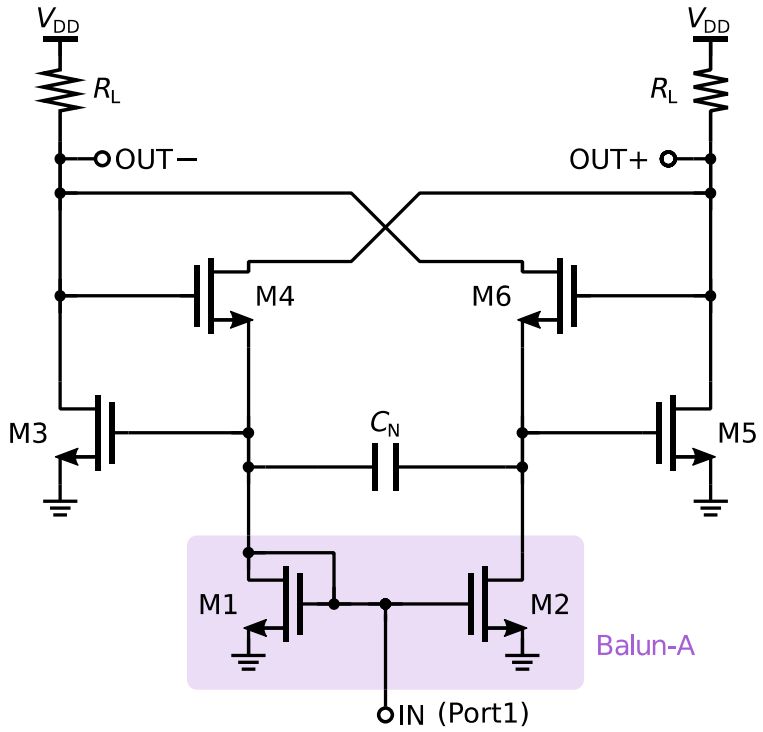


$$\beta_n = g_{m5}g_{m6} \cdot \frac{1}{(g_{m6} + G_A) + 2C_N s}$$

$$\beta_p = g_{m6} \cdot \frac{G_A + 2C_N s}{(g_{m6} + G_A) + 2C_N s}$$

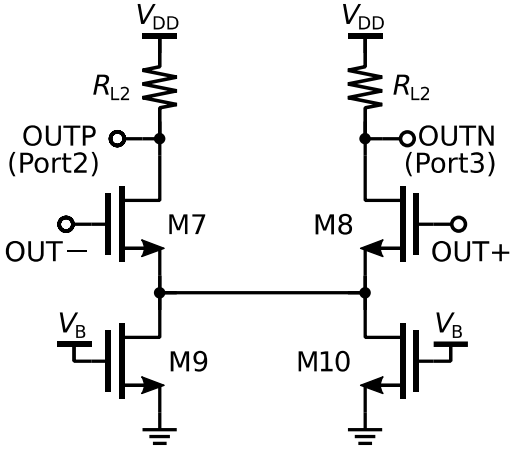
- C_N weaken β_n and strengthen β_p at high frequencies
- C_N improves not only GBWs but also CMRR!!

Design example



(a) Proposed active balun

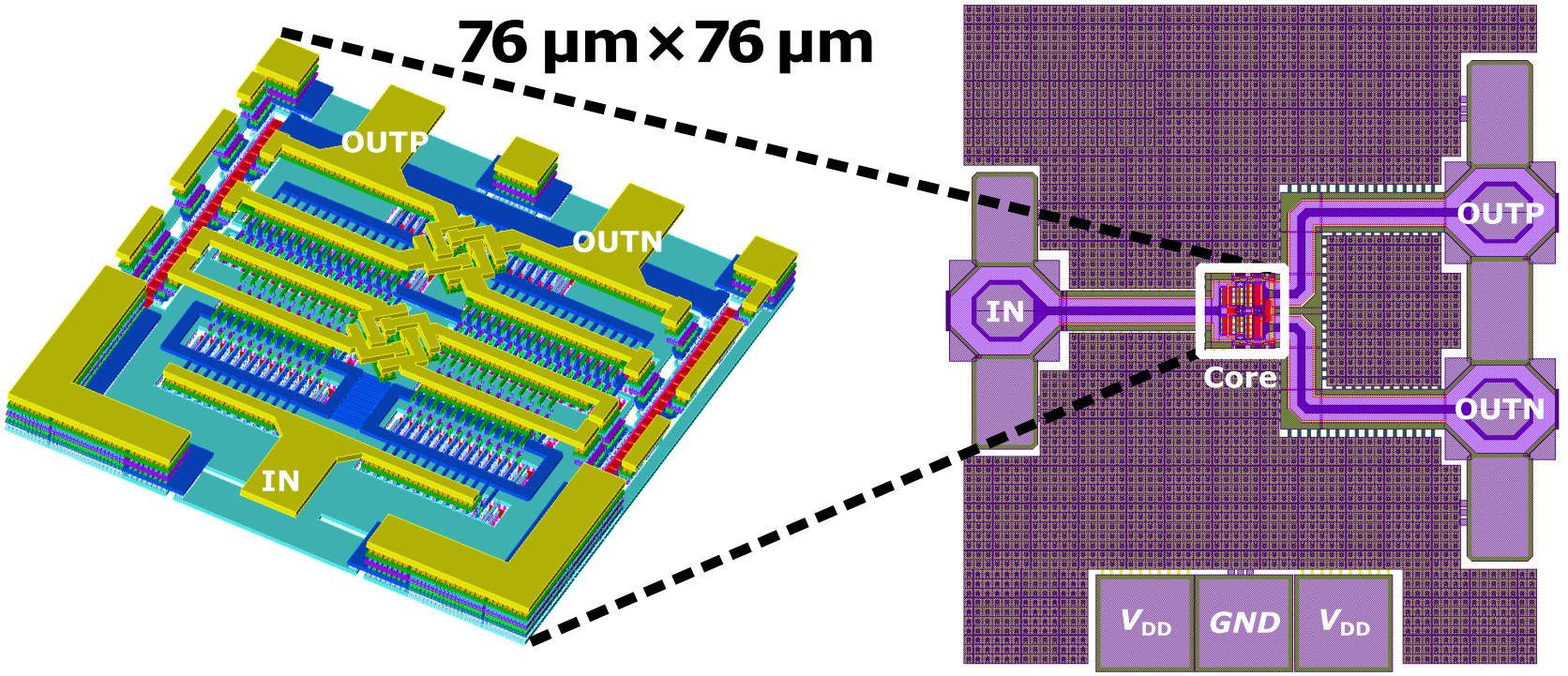
R_L	110 Ω
R_{L2}	55 Ω
M1 - M6	24 µm / 0.18 µm
M7 - M10	64 µm / 0.18 µm
C_N	22 fF
V_{DD}	2.2 V
V_B	1.0 V



(b) Output buffer

- Balun-A consists of a current mirror
- Output buffer improves the loop-gain R_L

Layout design

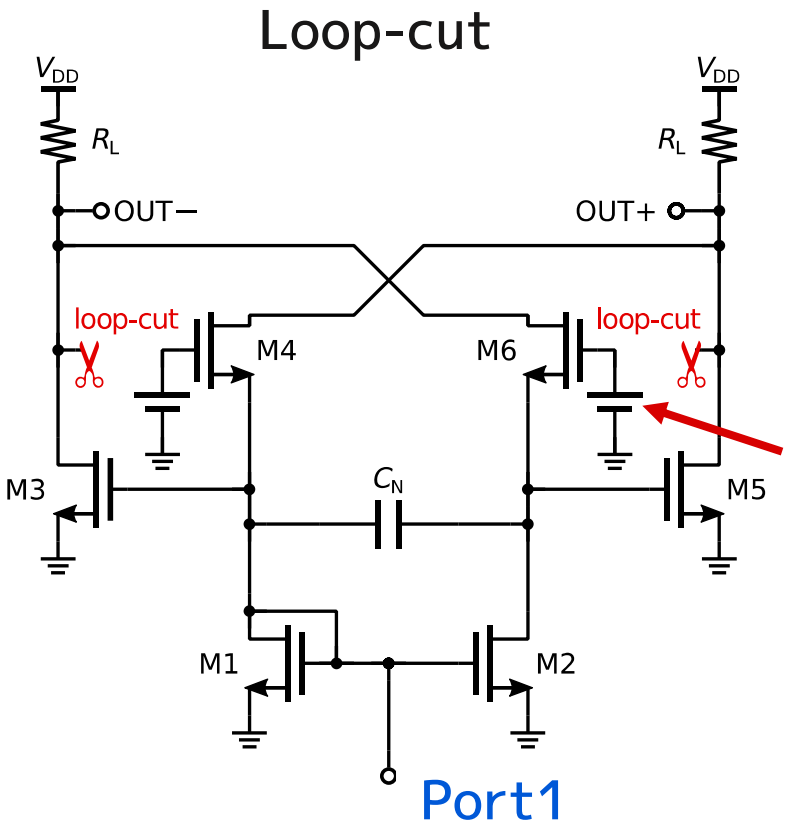


- Core area = 0.0058 mm^2 (Tiny!!)
- Symmetric layout using point symmetric cross-couples

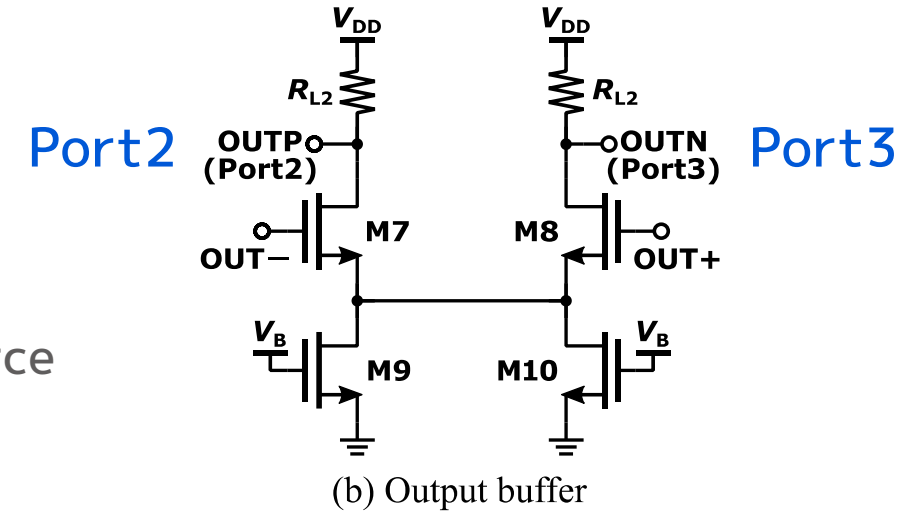
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Pre-layout simulation



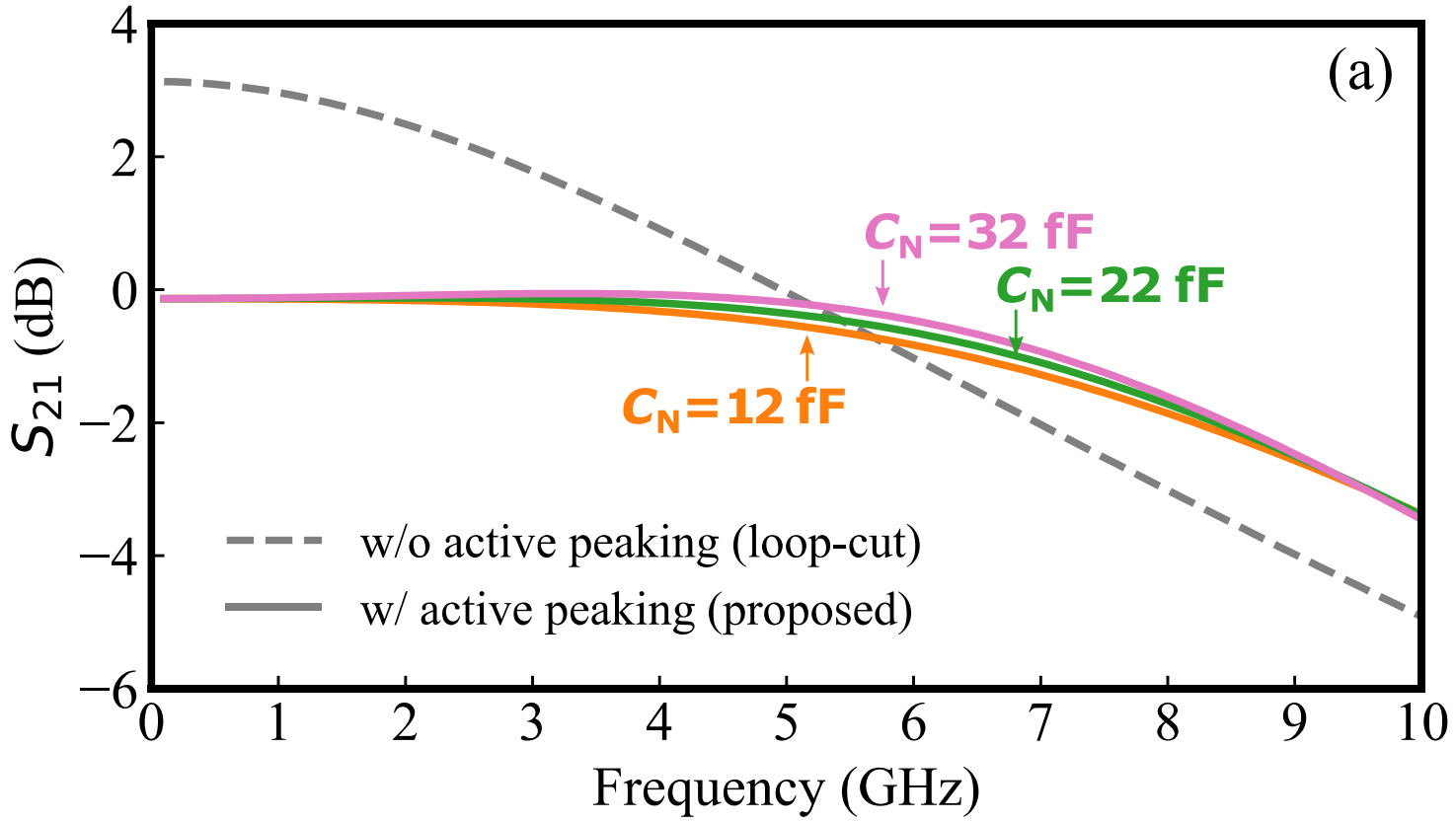
DC bias is fed
using voltage source



(b) Output buffer

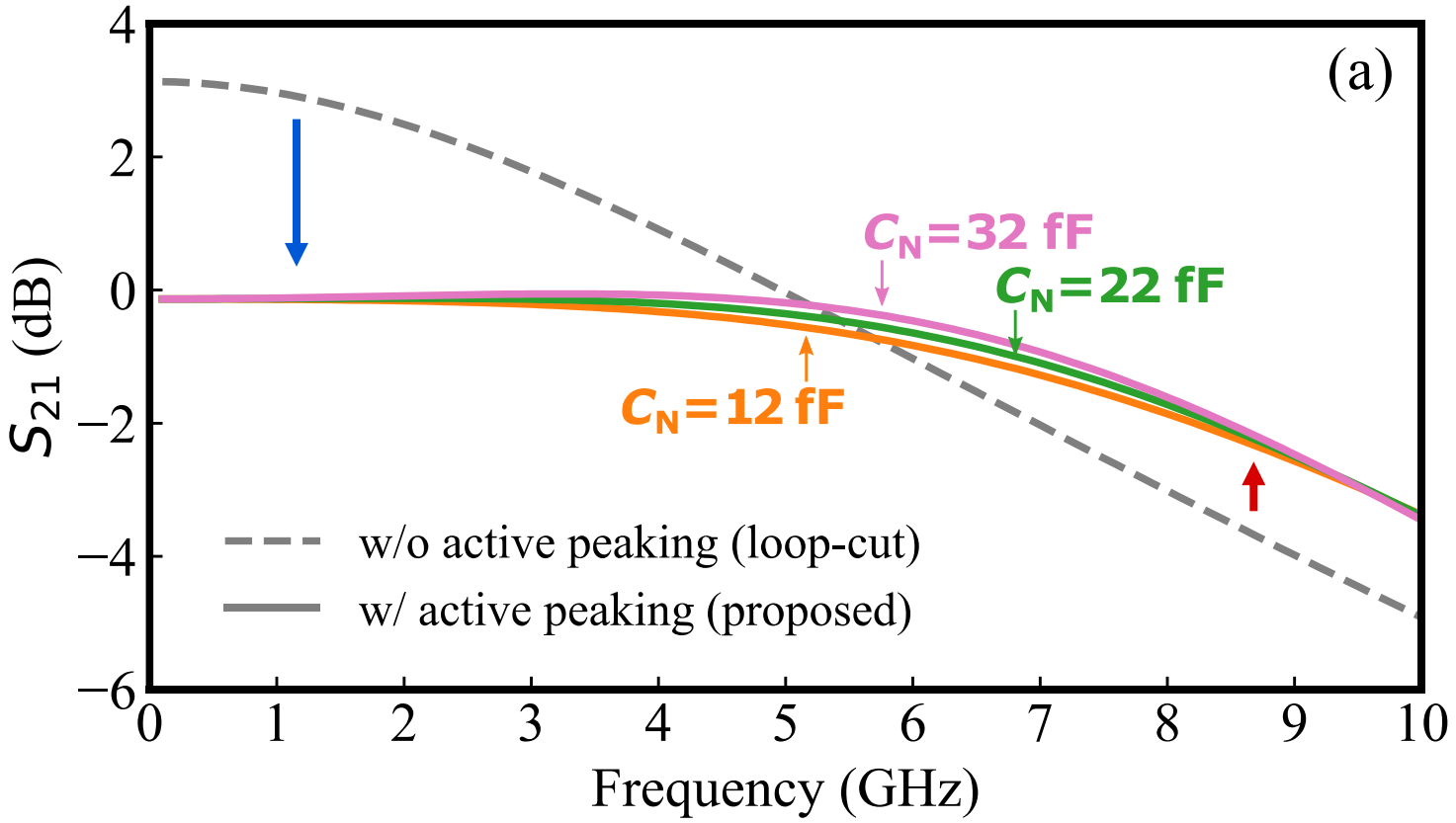
- To clarify C_N effects, the balun was parametrically simulated
- Loop-cut circuit was also simulated to assess GBW enhancement

Conversion gain S_{21}



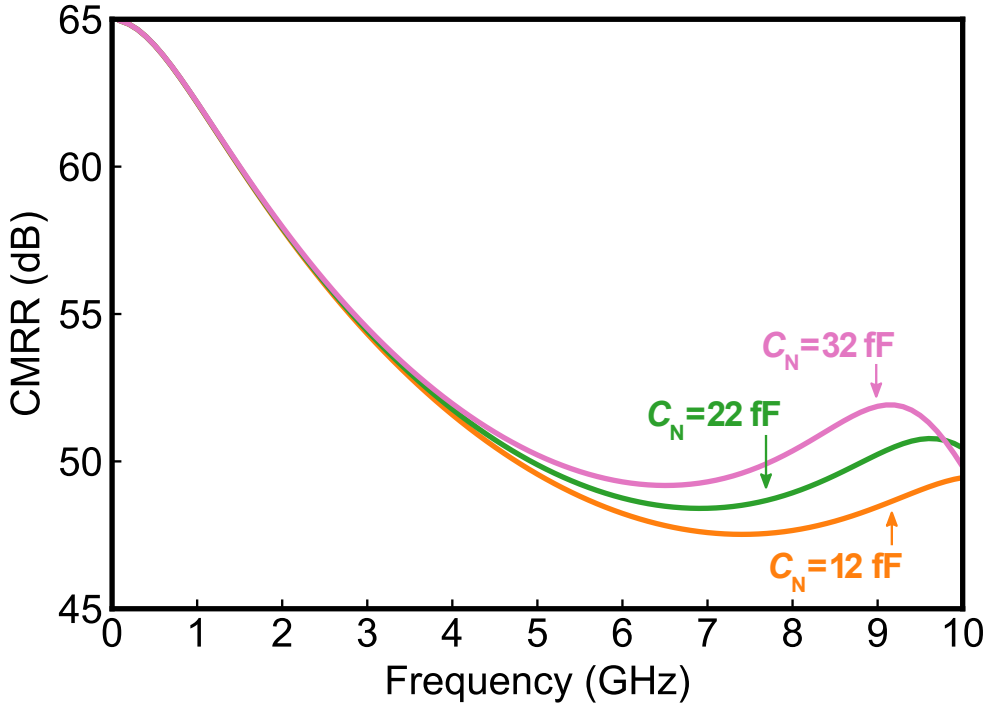
- Gain is decreased at Low freq. and increased at high freq.
- GBW is enhanced by 39% (Series peaking comparable!)

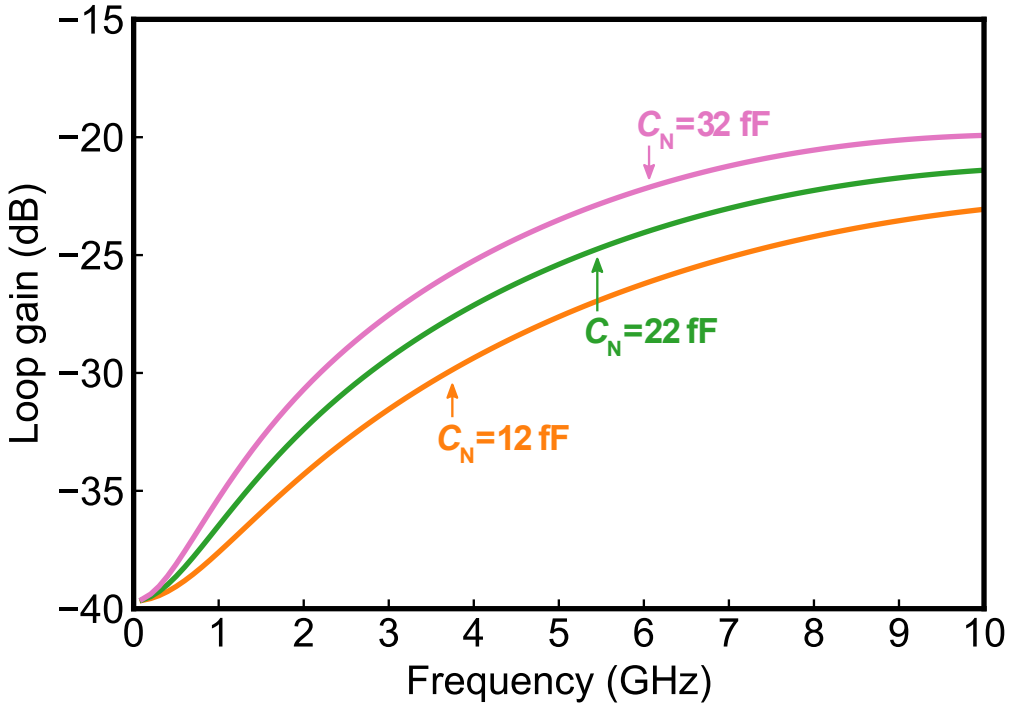
Conversion gain S_{21}



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CMRR vs. Loop gain

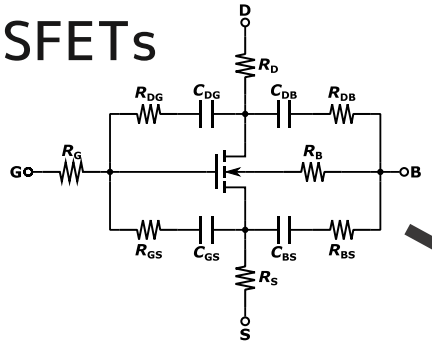


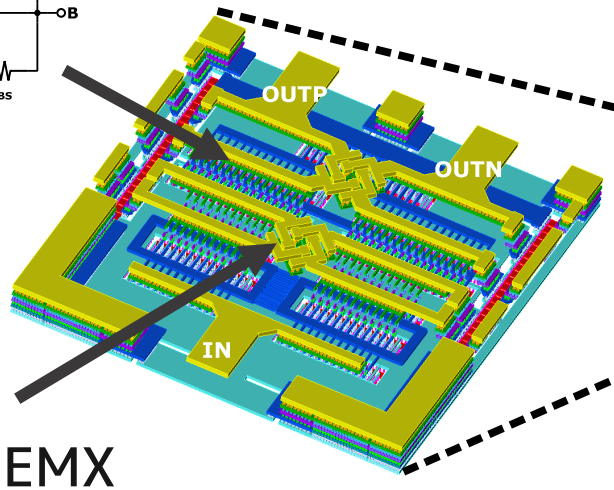


- Larger C_{N} improves the CMRR at high frequencies
- Larger C_{N} worsens the gain margin of the positive feedback

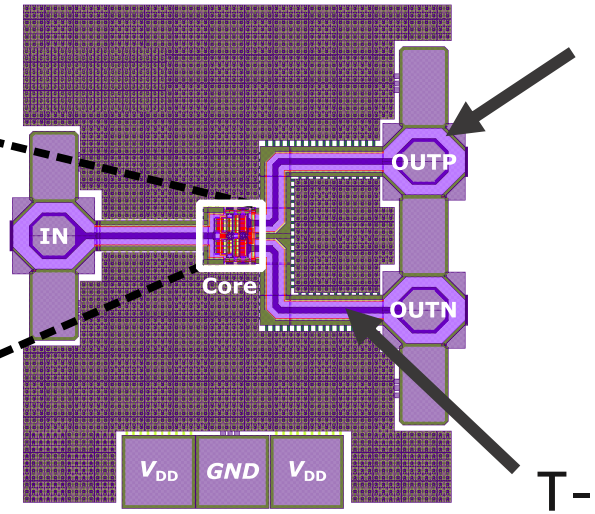
Post-layout simulation

MOSFETs

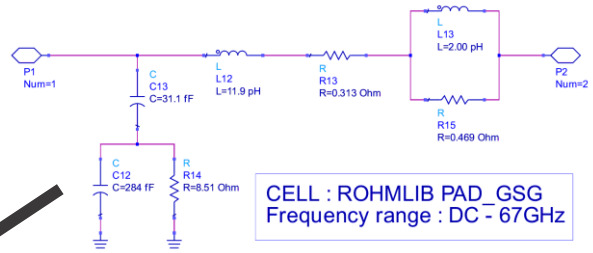




The internal wiring
was extracted with EMX



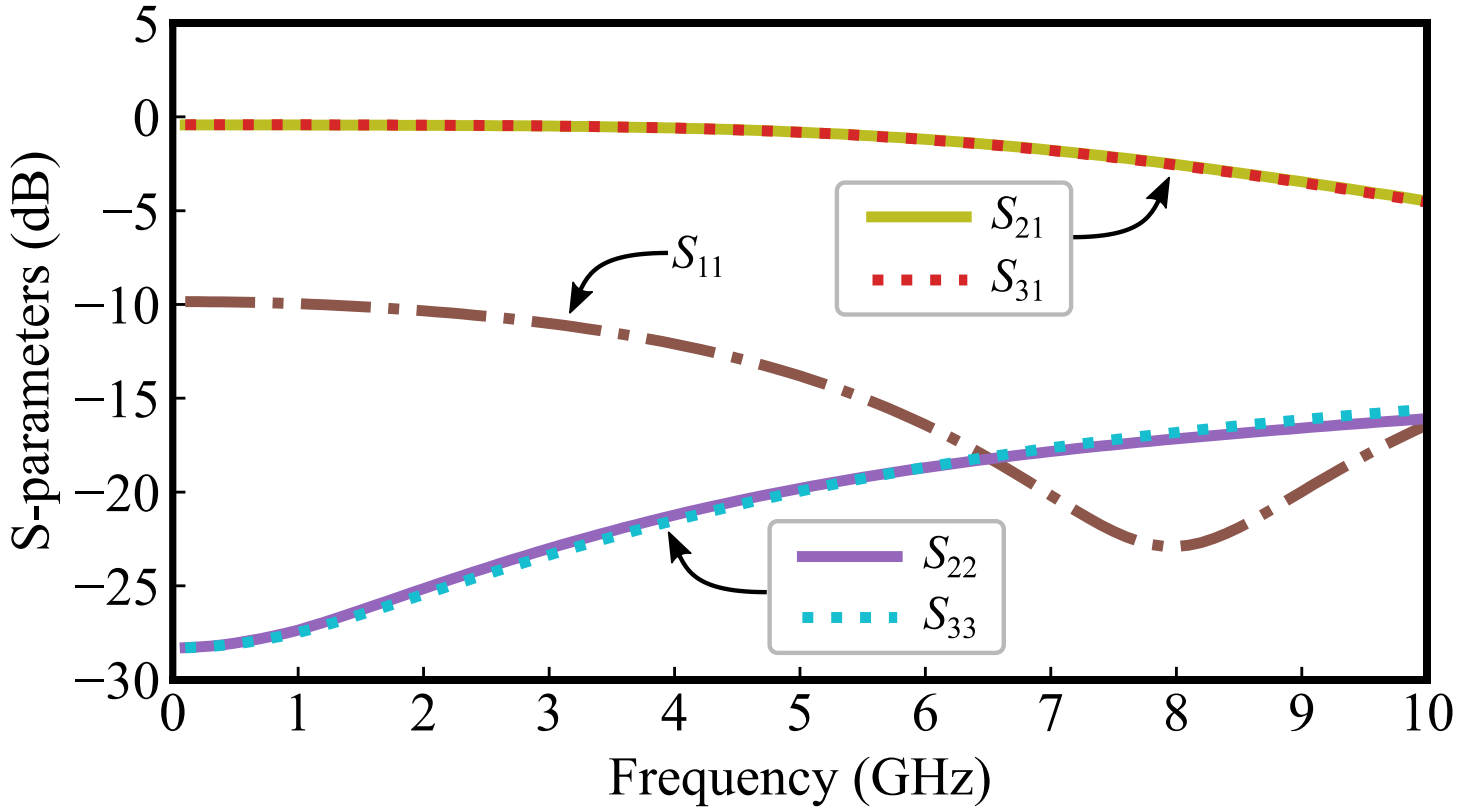
T-lines: RLGC table



RF-pads

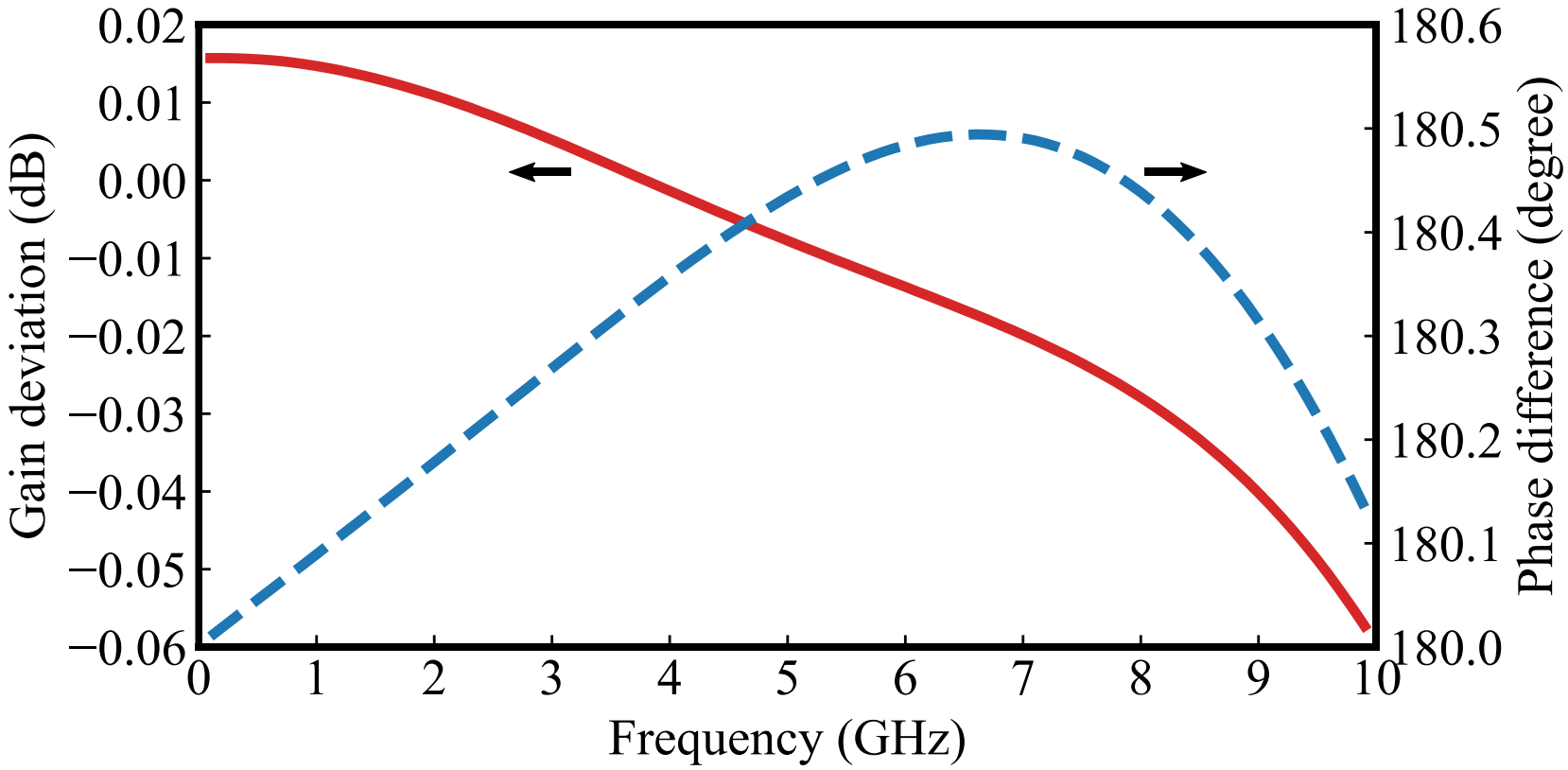
- Proposed balun was carefully simulated to predict losses
- Simulation includes almost all the parasitic elements

Simulated S-parameters



- Gain = -0.4 dB, bandwidth = 8.9 GHz
- Return losses are better than 9 dB across the bandwidth

Simulated deviations



- Gain deviation = 0.04 dB, Phase deviation = 0.5°
- These results do not include process variations

Comparison table

	This work (Simulated)	[2] MWCL 2009	[1] A-SSCC 2012	[3] MWCL 2016	[5] MOTL 2018
Technology	180 nm CMOS	130 nm CMOS	65 nm CMOS	180 nm BiCMOS	65 nm CMOS
Inductors or T-lines	Un-used	Used	Used	Used	Un-used
Core area (mm^2)	0.0058	0.37‡	0.26	0.11‡	0.0091
Bandwidth (GHz)	DC-8.9	2-40	53-65	DC-50	1-1.12
Gain deviation (dB)	0.04	0.5	0.36	1	1.4
Phase deviation	0.5°	10°	2.2°	10°	3.5°
Gain (dB)	-0.4	1	6.1	-0.8	4
IP1dB (dBm)	0.2	-5	N/A	-0.5	N/A
IIP3 (dBm)	12	N/A	N/A	7	N/A
Power (mW)	63.8	40	11.6	14.4	2.6

- Low deviations and broad bandwidth with a small core area !

Conclusion

- Trade-offs: accuracy ↔ speed ↔ area
- This work:
  - ✓Clarify the relation between CMRR and stability in the MPCCT
  - ✓Feedback loops in the MPCCT are available for the APT
  - ✓Additional capacitor improves not only GBWs but also CMRR
- Results:
  - ✓Low deviations, broad bandwidth, and tiny core area

CMRR > 45 dB　　DC - 8.9 GHz　　0.0058 mm^2

→ The proposed balun resolves the trade-offs.

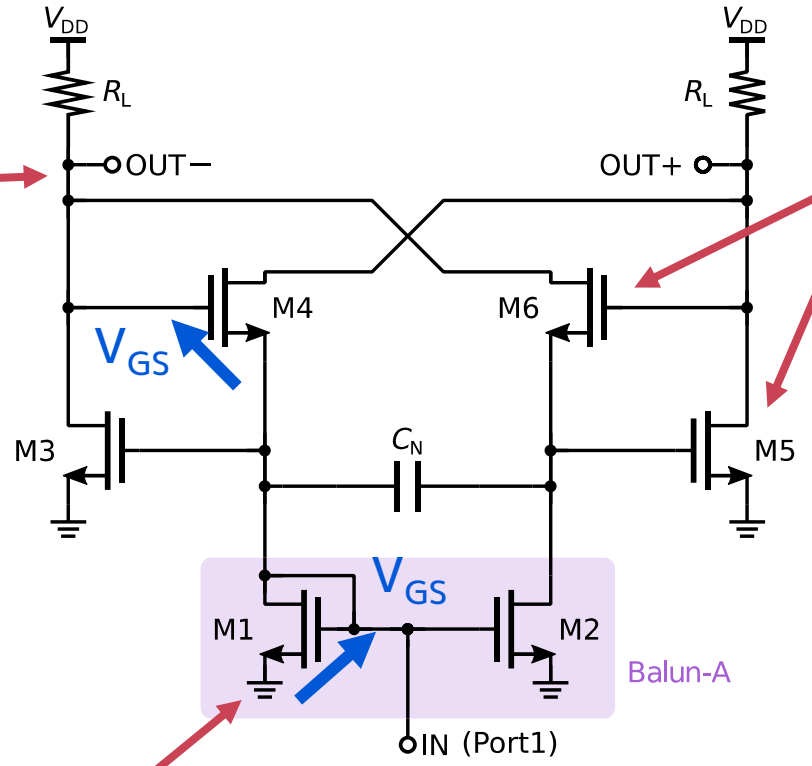
Acknowledgement

- This work was supported through the activities of VDEC, The University of Tokyo, in collaboration with Rohm Co., Ltd, Cadence Design Systems, Inc., Mentor Graphics, Inc., and Keysight Technologies, Inc.

Appendix

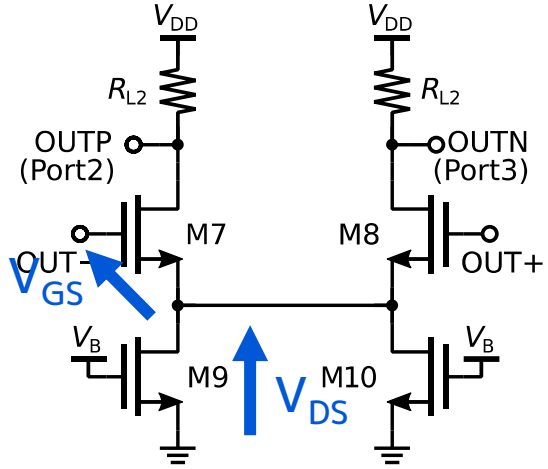
Why did you use a current mirror?

😄Output DC voltage is $2V_{GS}$,which ensure that all MOSFETs operate in the saturation region



(a) Proposed active balun

😄DC currents of the M1 to M6 are biased at same value, and it reduce the deviations



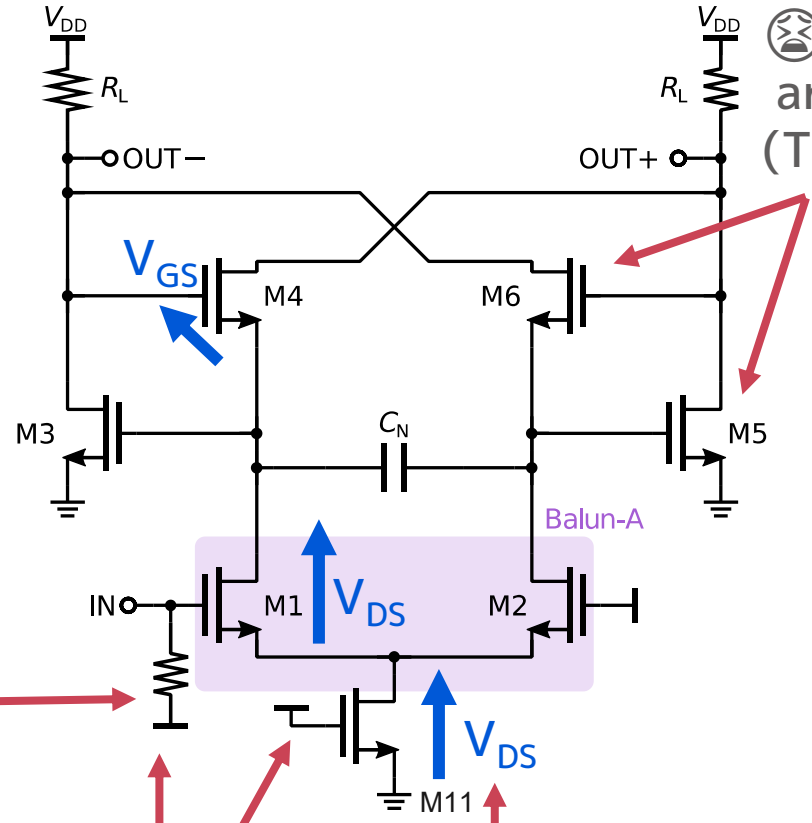
(b) Output buffer

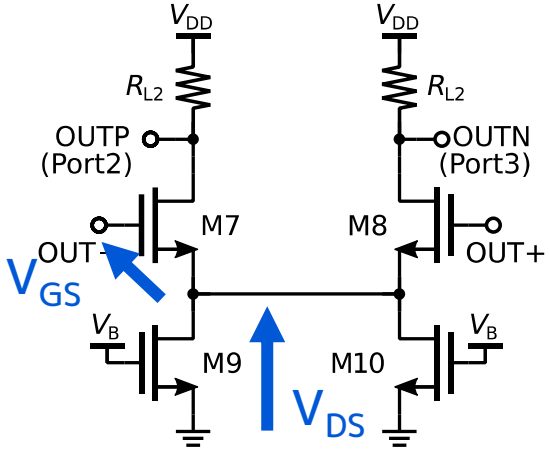
😄DC supply is not required ,which enable the balun to operate with a single power supply

😄Impedance matching is realized without using a resistor

Why not a differential pair?

😫Inconsistent of V_{DS} may causes the linear region operation





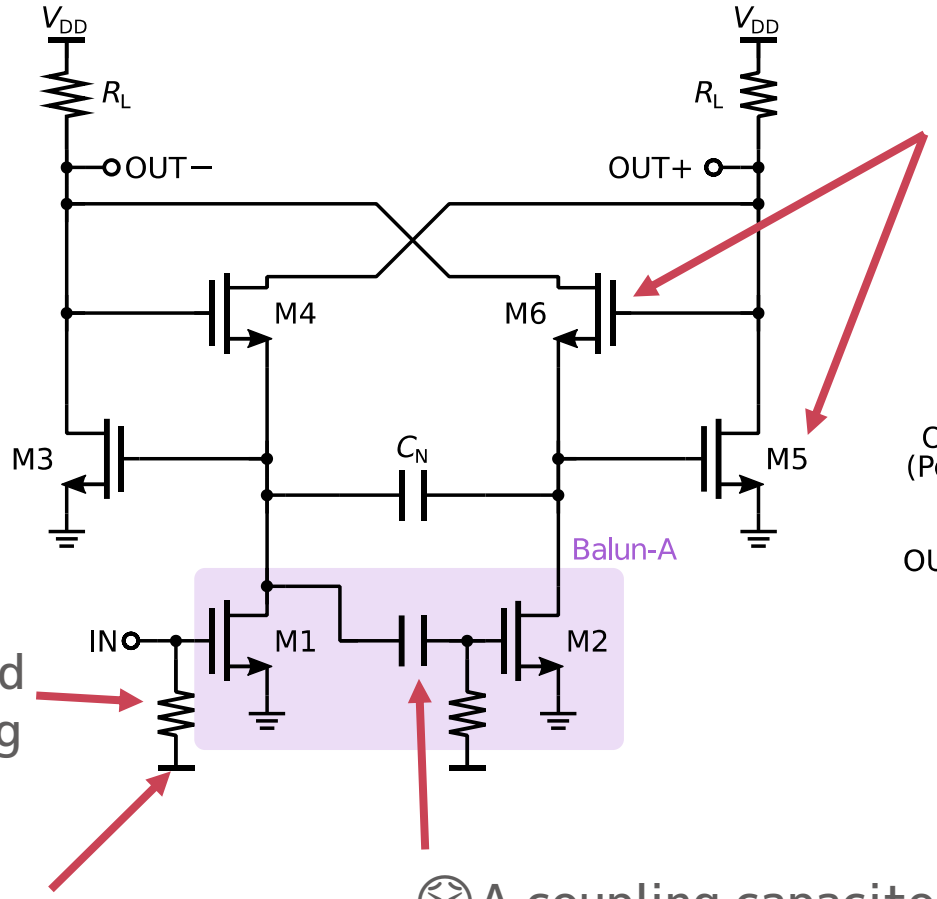
😫DC currents of the M5 and M6 are not the same value
(The same holds for the M3 and M4)

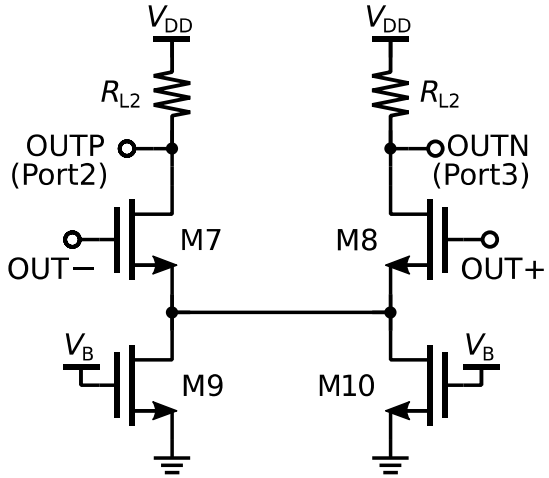
😫A resistor is required for impedance matching

😫Too many biases are required

😫A Tail current source wastes supply voltage

Why not a 2-stage CS amplifier?





😫DC currents of the M5 and M6 are not the same value
(The same holds for the M3 and M4)

😫A resistor is required for impedance matching

😫DC bias is required

😫A coupling capacitor is required for same bias current of the M1 and M2