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Design of an Area-Efficient Differential Distributed Amplifier Based on the Theory of Differential Transmission Lines

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Outline

1. Introduction
2. Analysis and design
   - Analysis of differential DAs
   - Modeling of inductors
   - Optimization of artificial T-lines
3. Simulation and result
   - Post-layout simulation
   - Comparison table
4. Conclusion

Outline

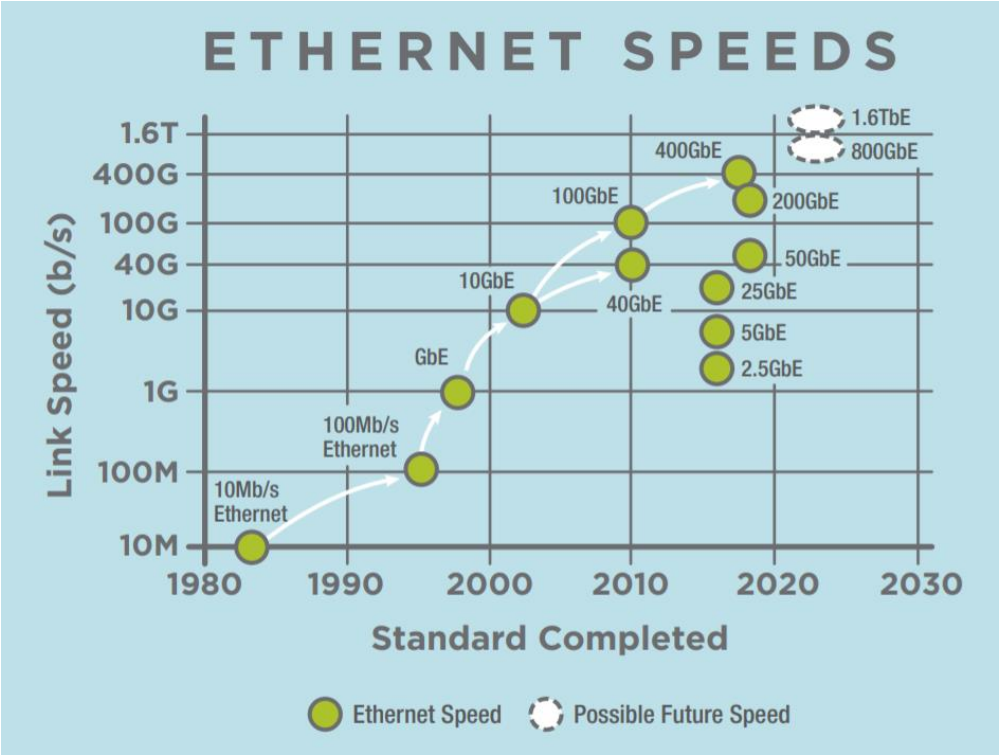
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Background

- Fiber-optic communications
- 400 GbE requirements
  - Over 25 Gbaud symbol rate
  - Over 12.5 GHz analog bandwidth

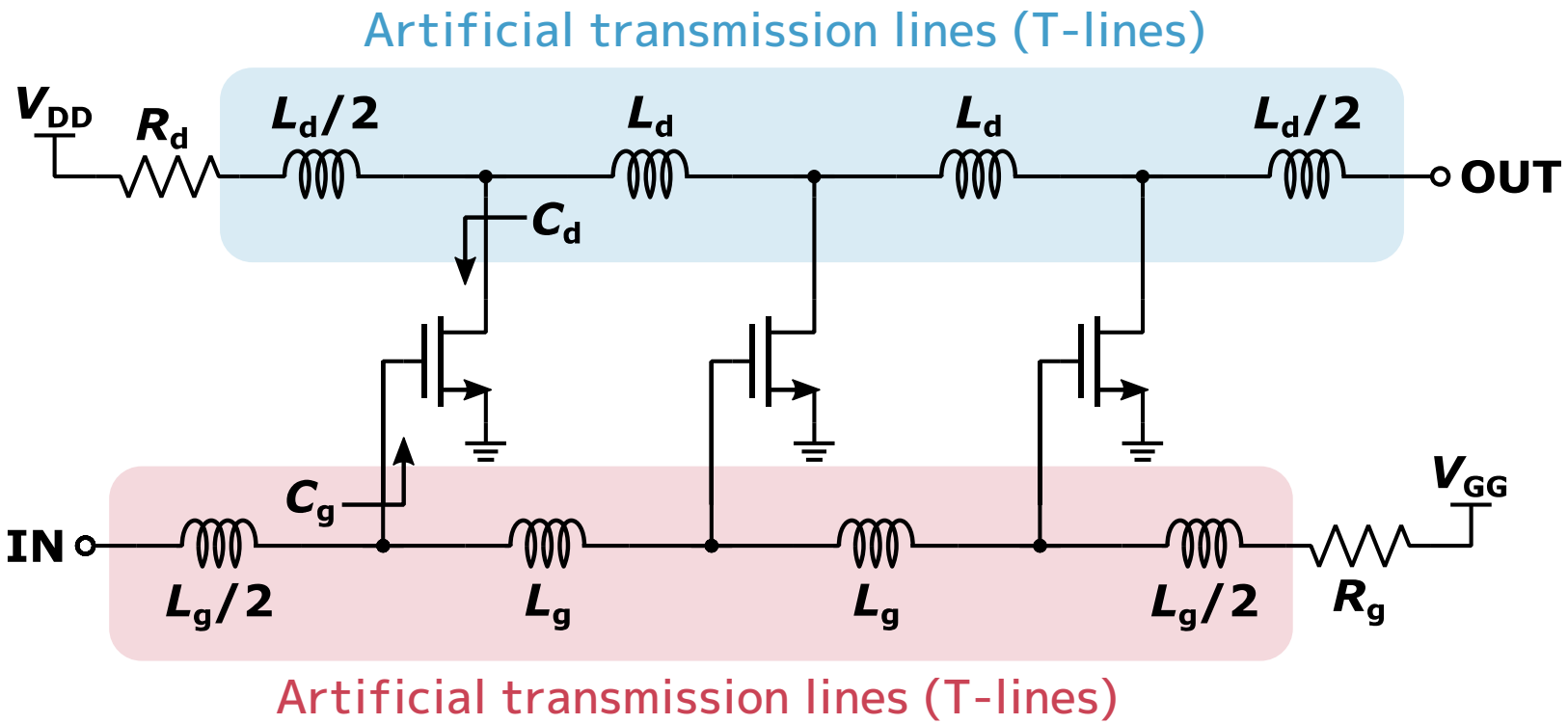
Expand bandwidth

Distributed amplifiers !



Ref. https://ethernetalliance.org/technology/2020-roadmap/

Distributed amplifiers (DAs)



- Cut-off frequency

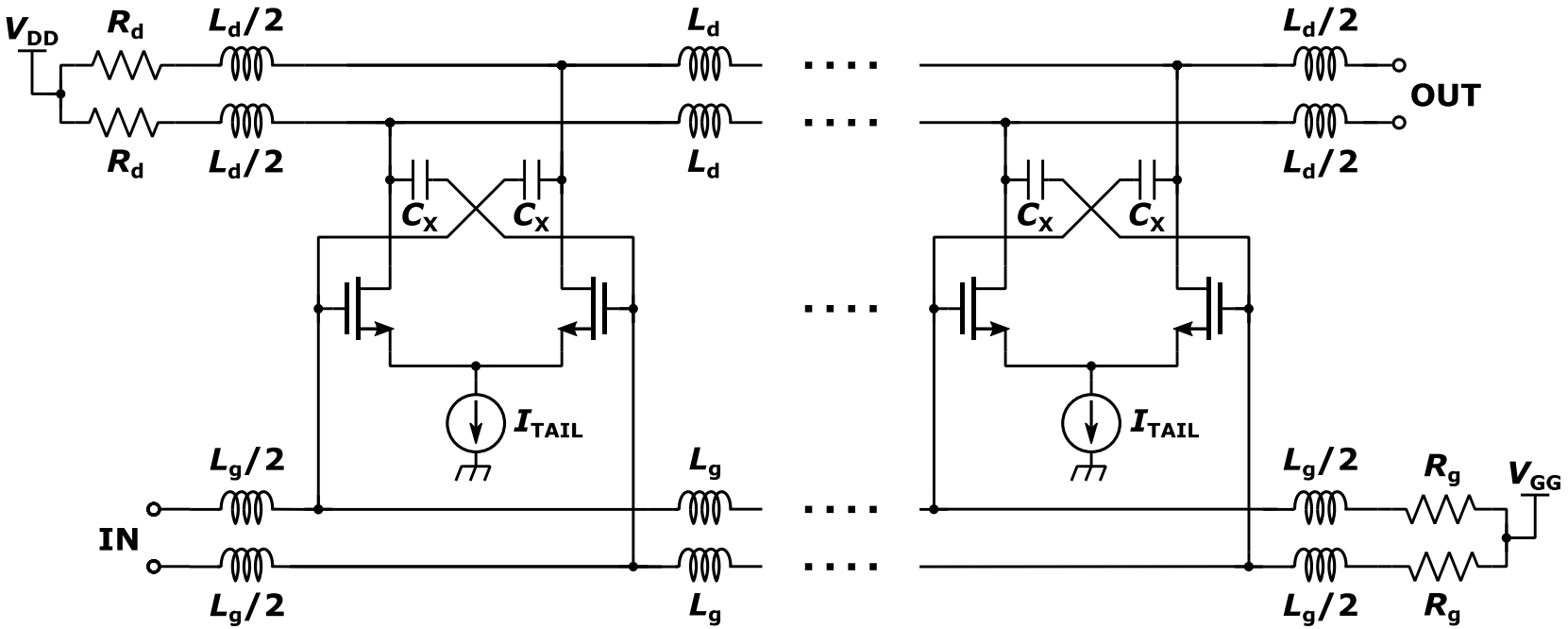
$$f_{Cg} = \frac{1}{\pi\sqrt{L_g C_g}}$$

- Characteristic impedance

$$Z_g = \sqrt{\frac{L_g}{C_g}}$$

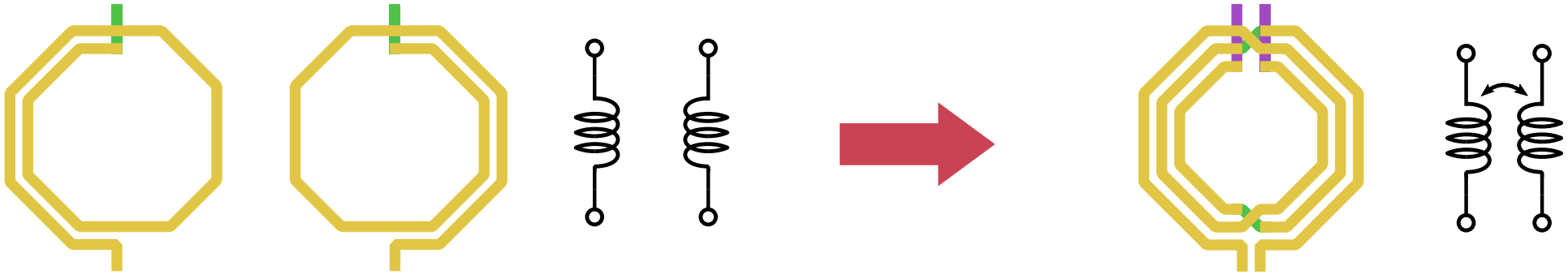
- Inductors and parasitic capacitors consists of T-lines:
  - Realize broadband characteristics
- Most of the conventional DAs are single-ended structure

Conventional differential DAs



- Many inductors
  - 😢 Increase the chip-areas and manufacturing costs
  - 😢 Complicate the wiring

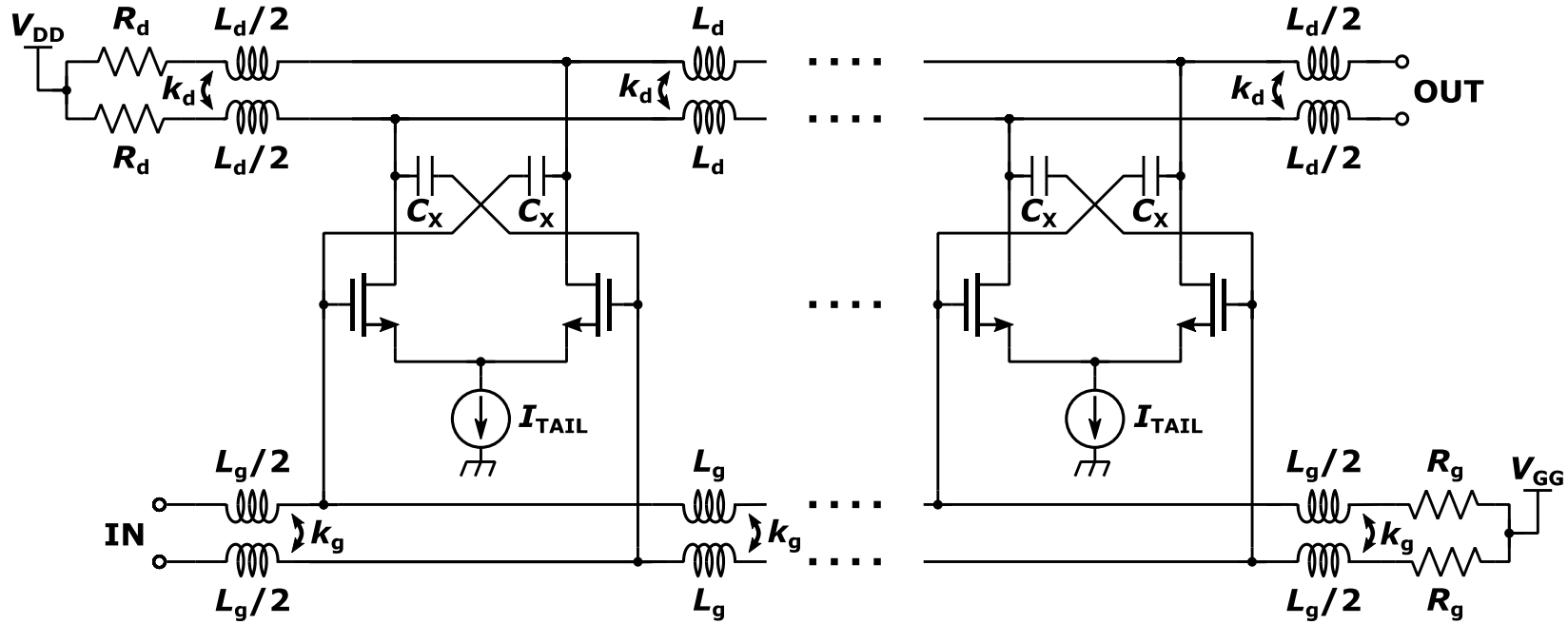
Coupled inductors



Un-coupled inductors　　Coupled inductors

- Inductive coupling is often used to reduce the areas
- Use cases:
  - Low noise amplifiers (J. J. Zhou et al., *J.SSC*, 1998)
  - Laser drivers (T. Kuboki et al., *CICC*, 2010)
  - Distributed transversal filters (J. Sewter et al., *J.SSC*, 2006)

Diff. DAs using coupled inductors

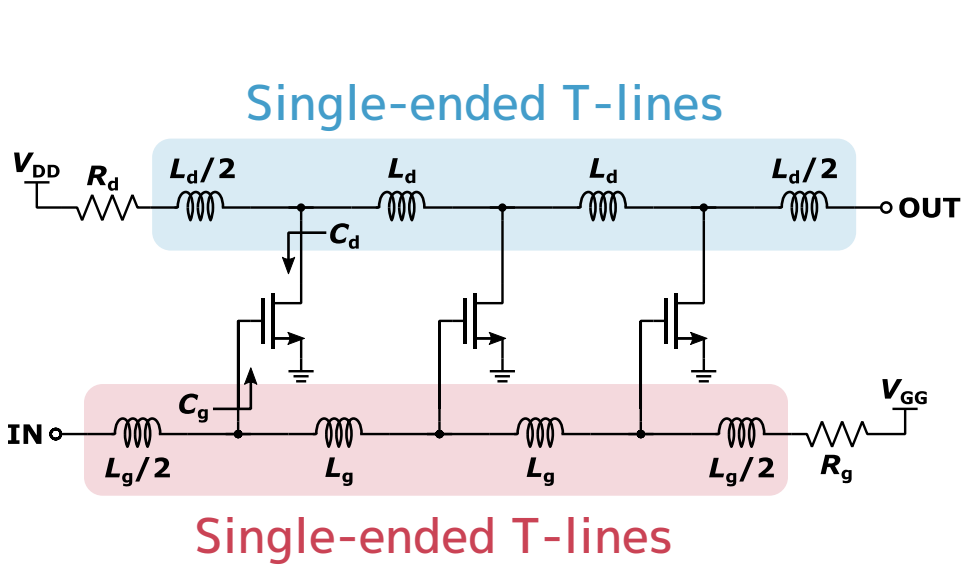


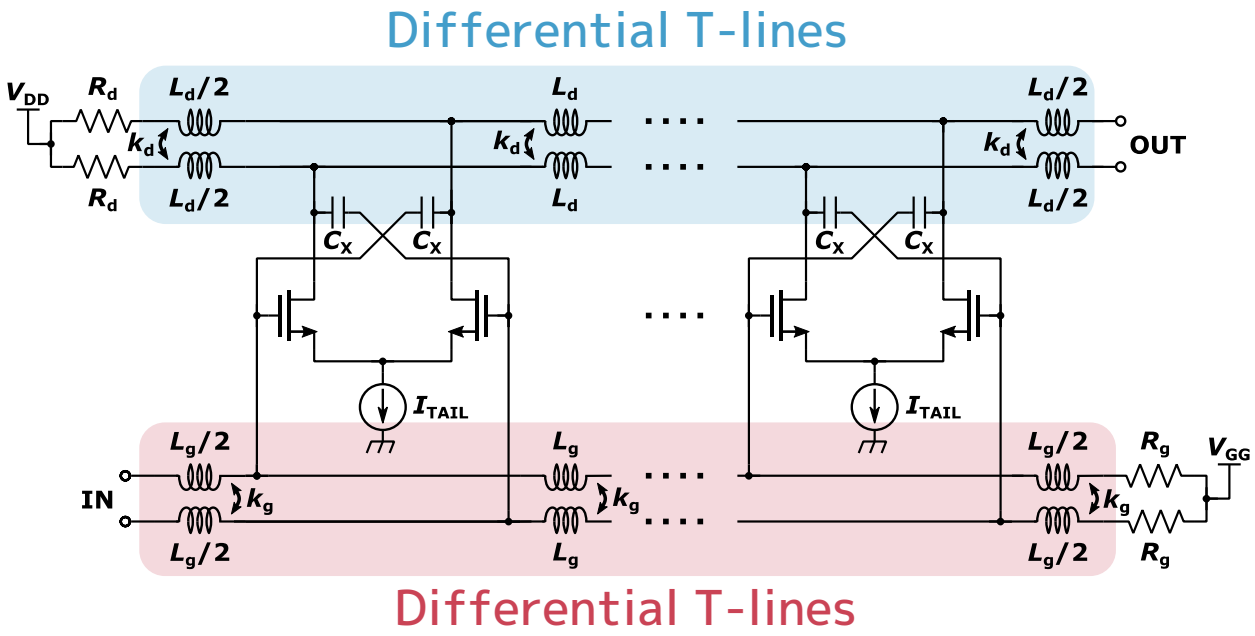
- Coupled inductors reduce the area and simplify the wiring
- Mutual coupling need to be considered
- Research target : Establish a systematic design method
  - Analysis → Modeling → Optimization

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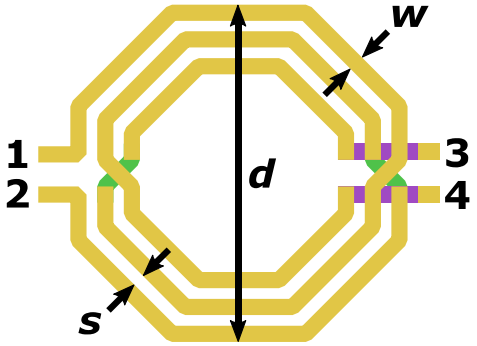
Analysis of the differential DAs



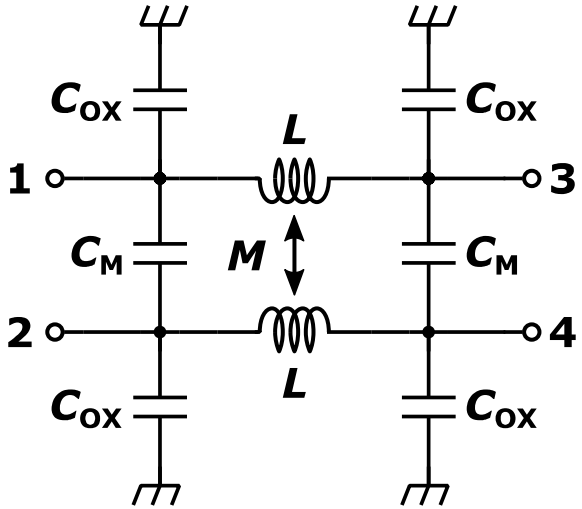


- Single-ended DAs are composed of single-ended T-lines
- Differential DAs are also composed of differential T-lines
  - Mutual inductance and capacitance need to be modeled

Model of the coupled inductors



Layout



Loss-less model

- Parameters:
  - L : self-inductance
  - M : mutual inductance
  - C_{OX} : oxide capacitance
  - C_M : mutual capacitance
- All resistors are neglected for simplified analysis

Scalable modeling

① Electromagnetic analysis

4-port Y-parameters

② Parameter extraction

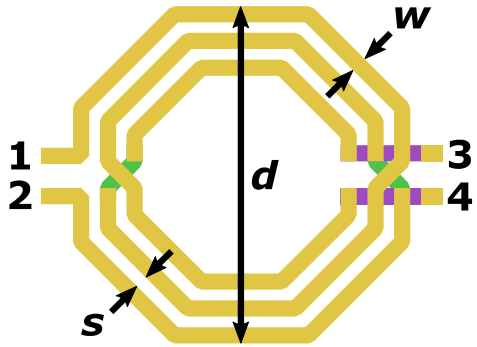
$$L = \frac{\mathrm{Im}(Y_{31})}{\omega \mathrm{Im}(Y_{31})^2 - \omega \mathrm{Im}(Y_{41})^2}$$

③ Polynomial approximation

$$L(d,s,w) = \alpha_0 d^2 + \alpha_1 s^2 + \alpha_2 w^2 + \alpha_3 ds + \alpha_4 dw + \alpha_5 sw + \alpha_6 d + \alpha_7 s + \alpha_8 w + \alpha_9$$

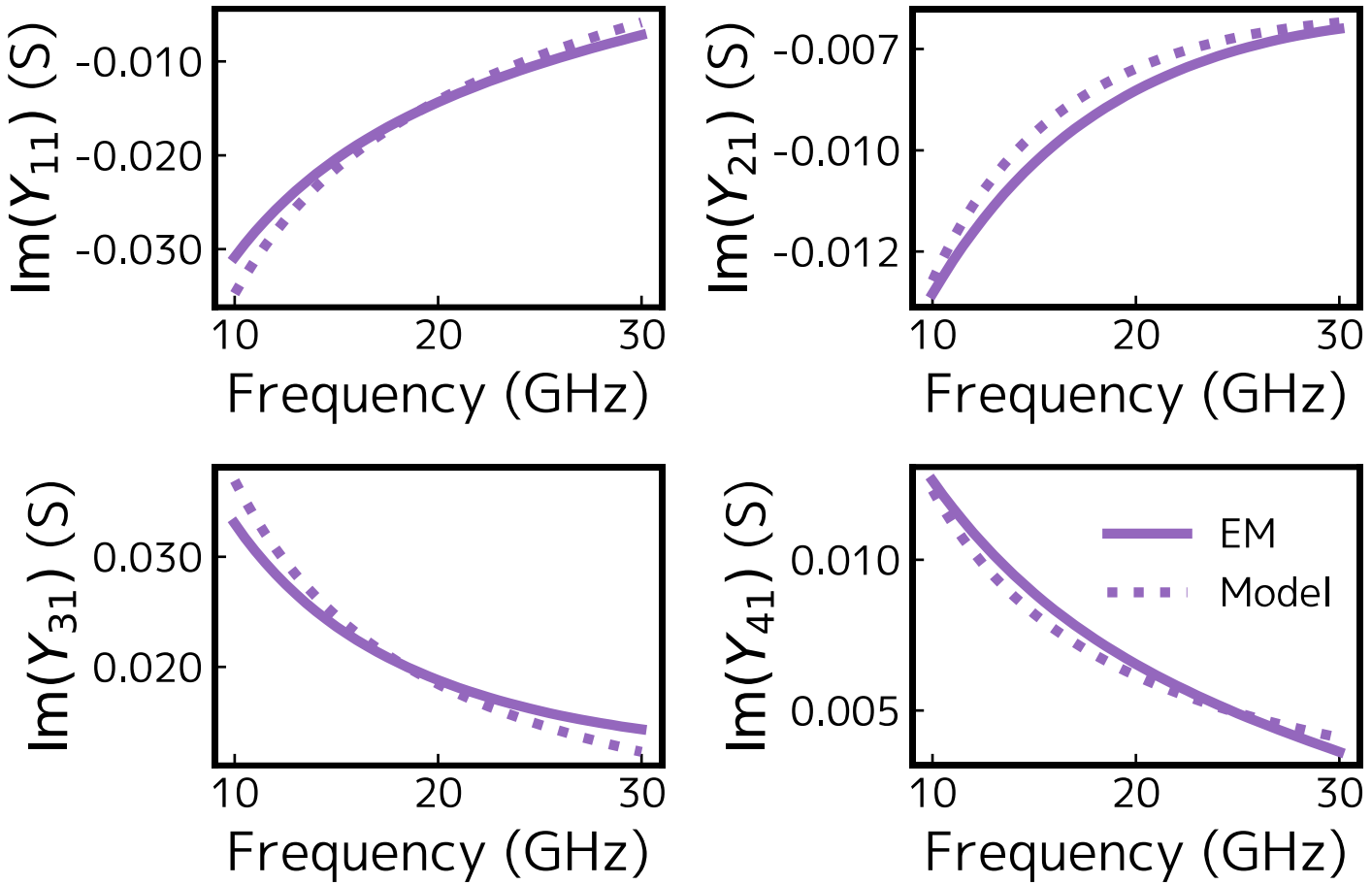
Specifications of EM analysis

Dimensions	Values
d (μm)	90, 110, 130, 150
s (μm)	2, 5, 7, 10
w (μm)	2, 4, 6
Number of turns	2.5 (Both primary and secondary turns)



Dimensions

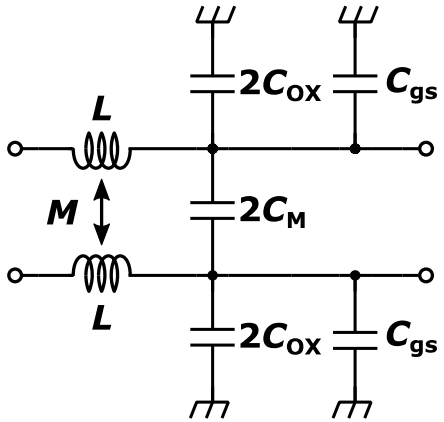
Fitting results



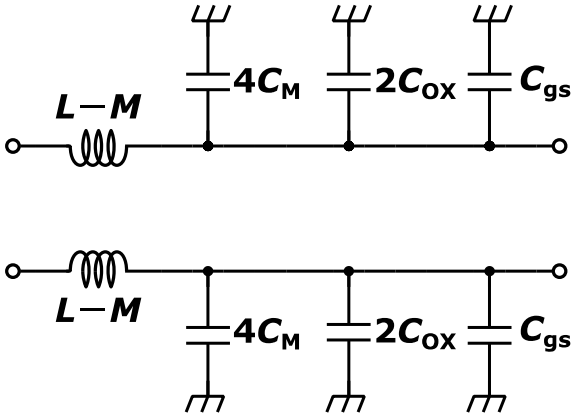
at
d=120 μm
s=6 μm
w=5 μm

- Good fitting from 10 GHz to 30 GHz

Analysis of the differential T-lines



Equivalent of the gate-line per section



Odd-mode equivalent

- Odd-mode impedance :

$$Z_{g_{odd}} = \sqrt{\frac{L-M}{4C_M + 2C_{OX} + C_{gs}}}$$

- Phase velocity :

$$v_{g_{odd}} = \frac{1}{\sqrt{(L-M)(4C_M + 2C_{OX} + C_{gs})}}$$

- Cut-off frequency :

$$f_{C_g} = \frac{v_{g_{odd}}}{\pi}$$

Optimization procedure

① Gate line optimization

$$\max f_{C_g} \cap \min |Z_{g_{odd}} - 50|$$

Maximize bandwidth & impedance matching

② Drain line optimization

$$\min |v_{g_{odd}} - v_{d_{odd}}| \cap \min |Z_{d_{odd}} - 50|$$

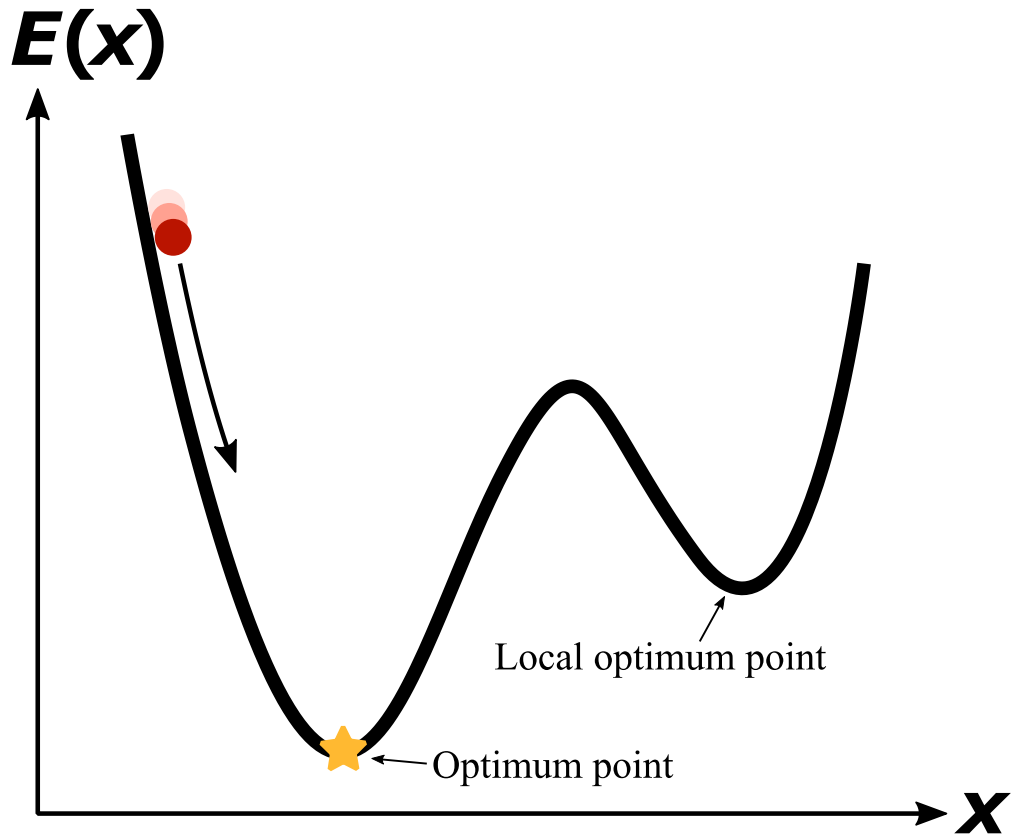
Velocity matching & impedance matching

✓ Optimize the gate line before the drain line because $C_{gs} > C_{ds}$

✓ Gate and drain can be optimized separately because the cross-coupled capacitors neutralize C_{dg}

Optimization method

- Gradient descent algorithm:
  - Find an optimum point
    like a ball rolling down a hill
- To avoid local optimum points:
  - Change the variables randomly
    every 100 steps



Gate line optimization

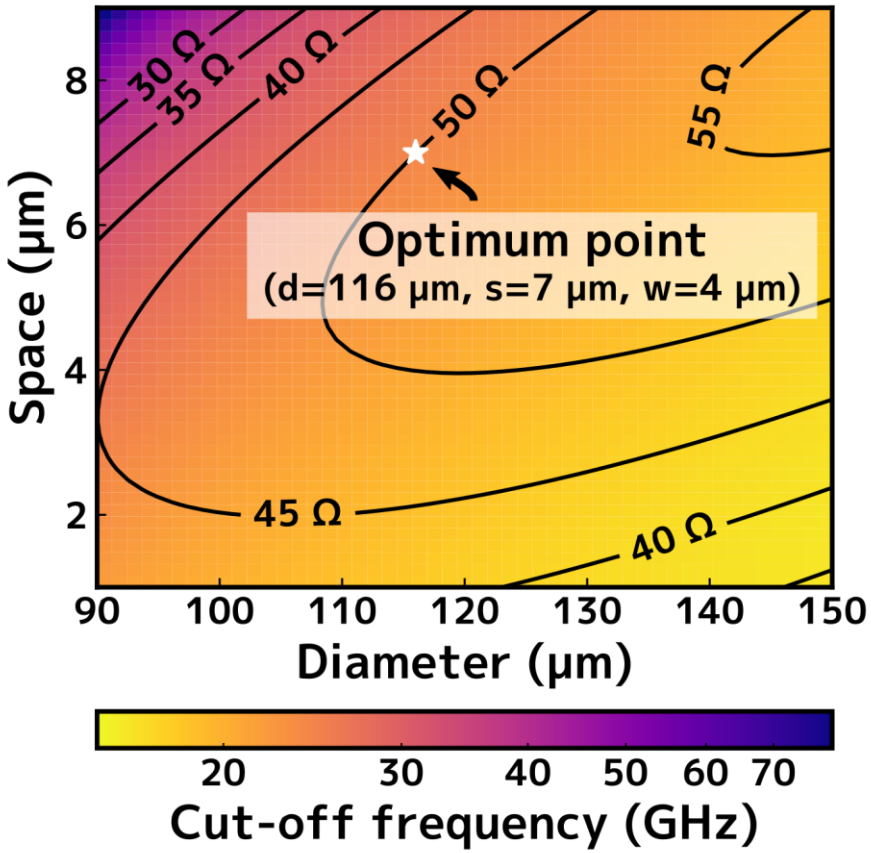
- Evaluation function:

$$E_g(d, s, w) = \zeta_0 \left(Z_{g_{odd}} - 50\right)^2 - \zeta_1 f_{C_g}$$

Impedance matching Maximize bandwidth

※ ζ_0 and ζ_1 are weighting factors

- Optimization results:
  - $d = 116$ μm, $s = 7$ μm, and $w = 4$ μm
  - $Z_{g_{odd}}$ = 50.0 Ω
  - f_{C_g} = 24.5 GHz



Optimization result

Drain line optimization

Evaluation function:

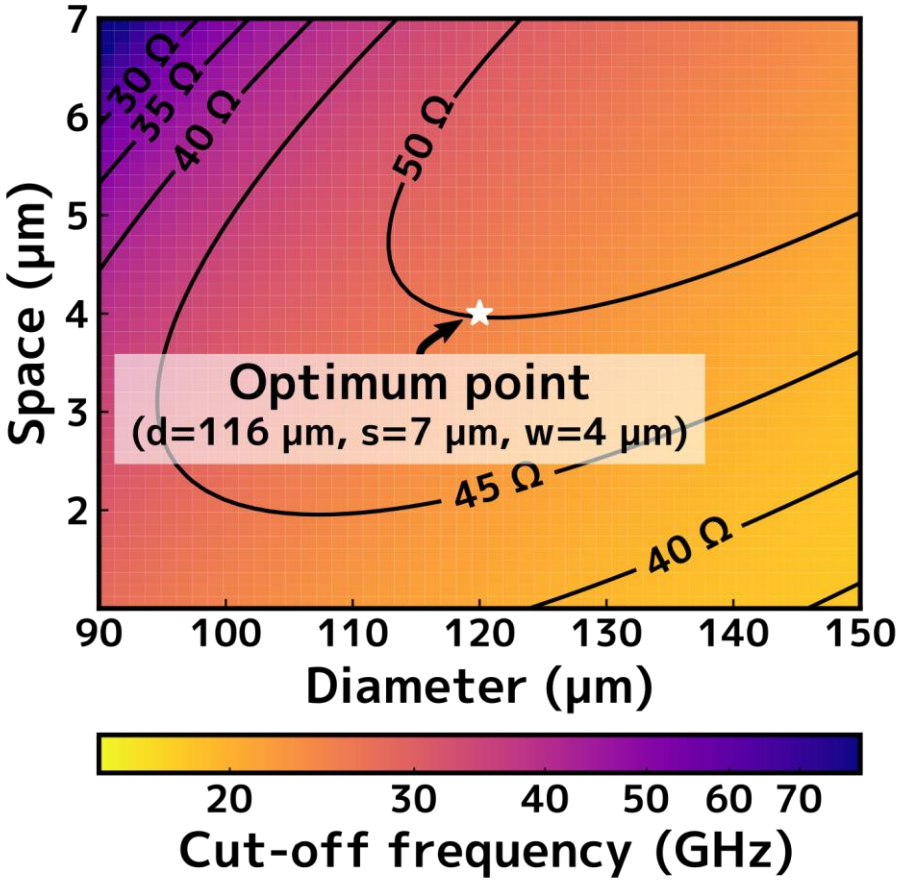
$$E_{\mathrm{d}}(d,s,w) = \eta_0\left(Z_{\mathrm{d_{odd}}} - 50\right)^2 + \eta_1\left(v_{\mathrm{d_{odd}}} - v_{\mathrm{g_{odd}}}\right)^2$$

Impedance matching　Velocity matching

※ η_0 and η_1 are weighting factors

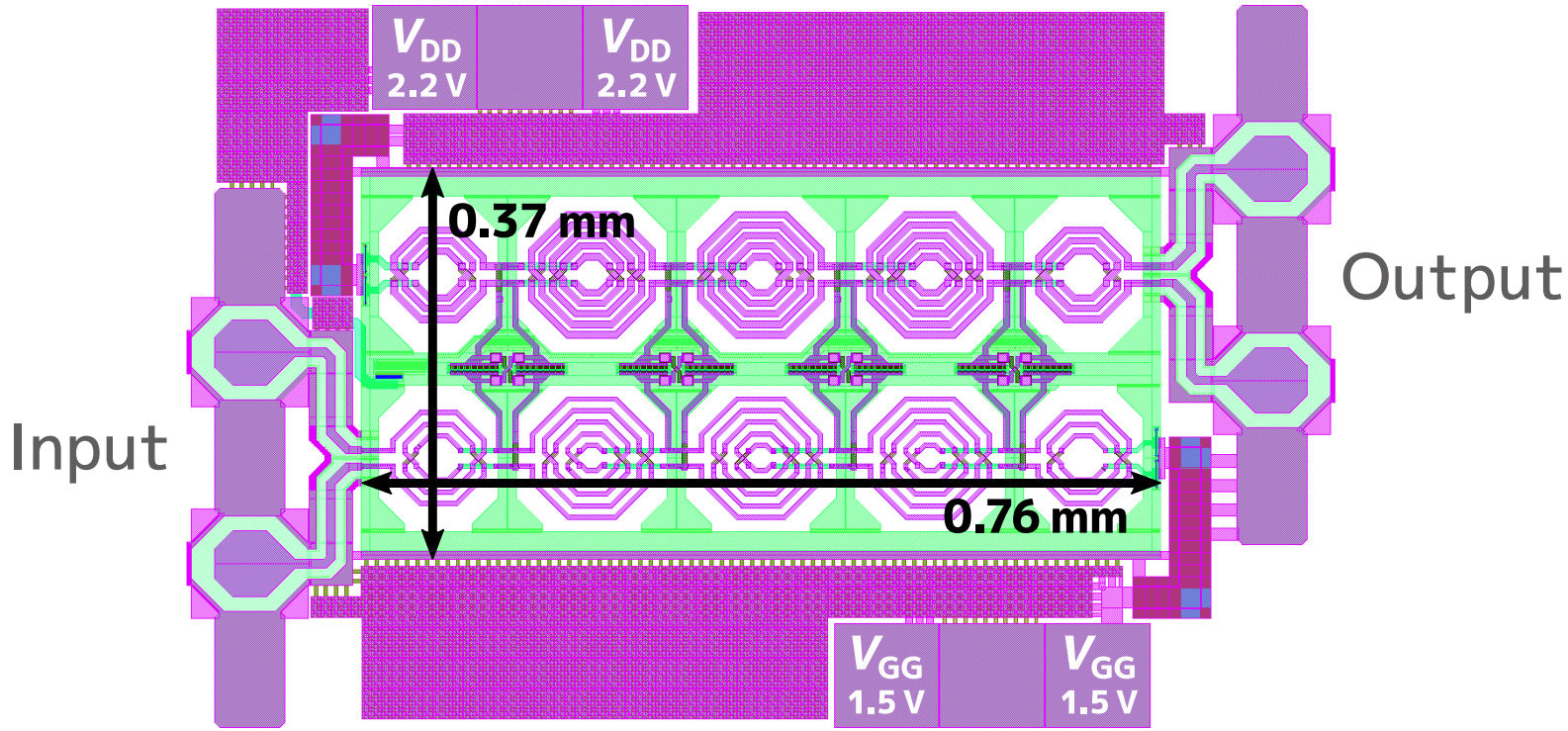
Optimization results:

- $d = 120$ μm, $s = 4$ μm, and $w = 6$ μm
- $Z_{\mathrm{d_{odd}}}$ = 50.1 Ω (0.2% error)
- $f_{\mathrm{C_d}}$ = 24.9 GHz (2% error)



Optimization result

Layout

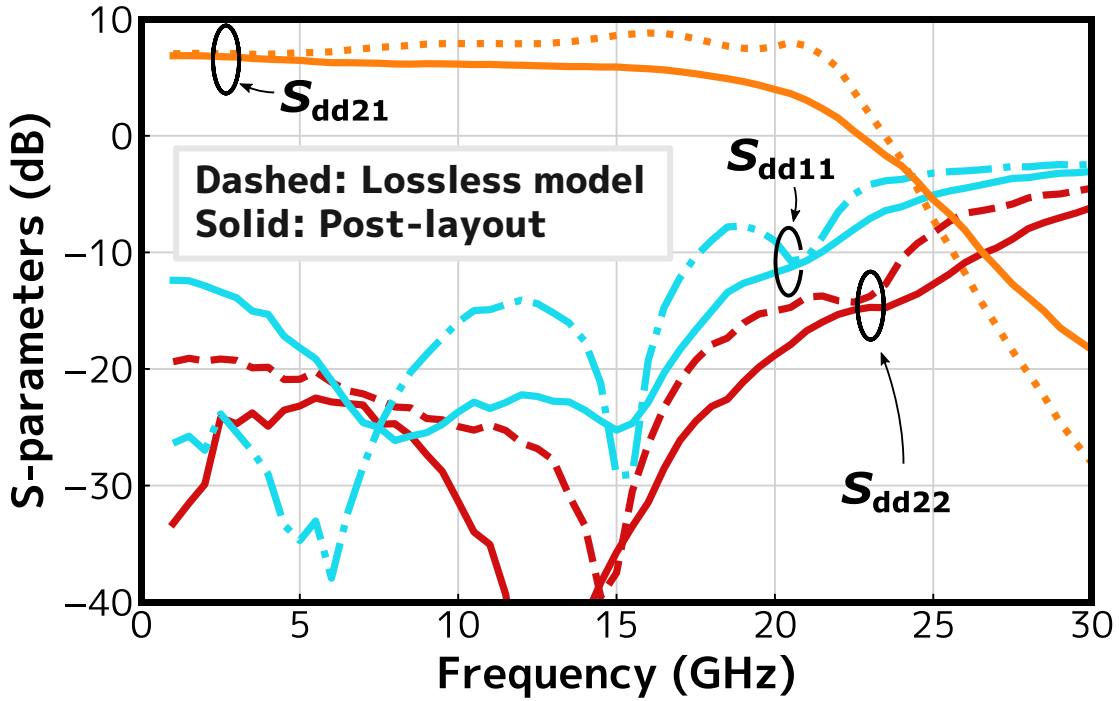


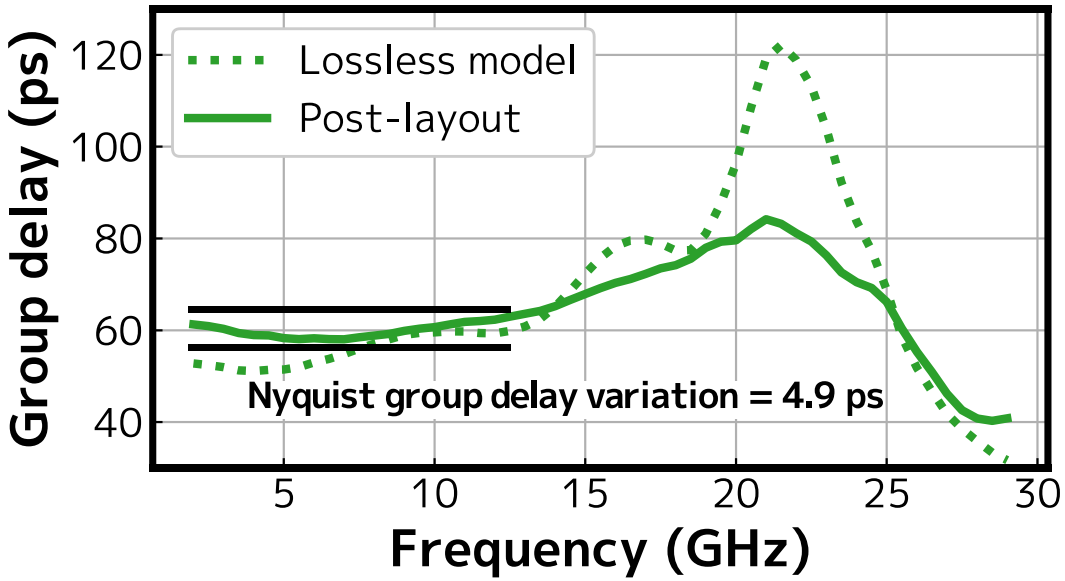
- 1P5M 180 nm standard CMOS technology
- Core area of 0.28 mm^2

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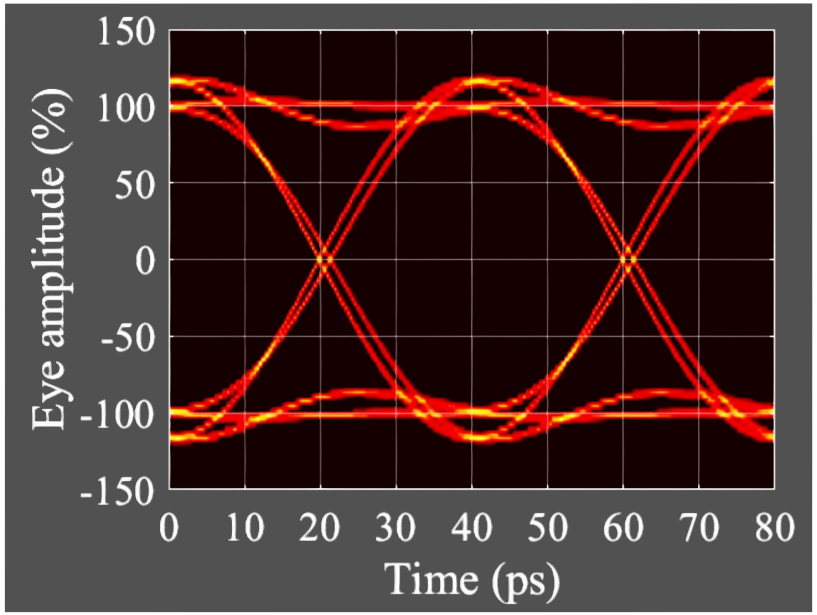
S-parameter simulation results



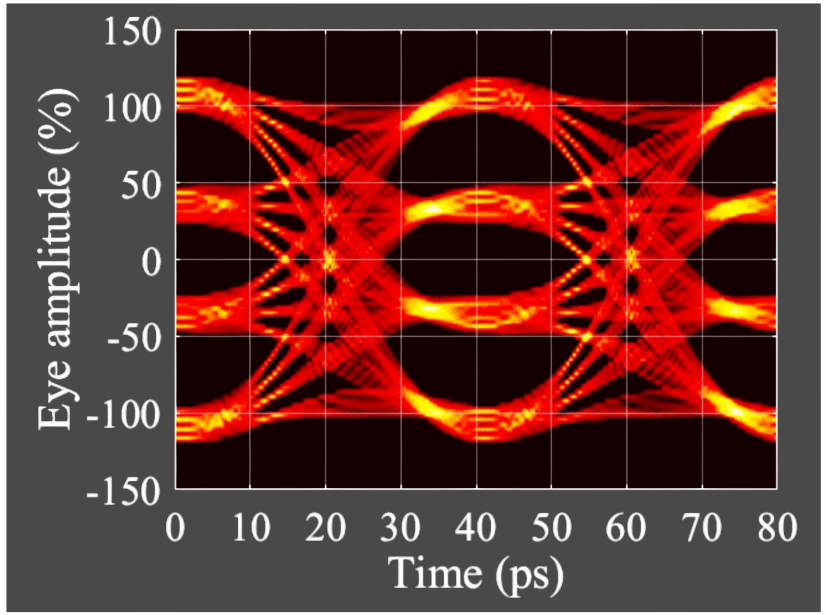


- Bandwidth of 20.2 GHz
  - 18% smaller than the theoretical bandwidth of 24.5 GHz
- Nyquist group delay variation of 4.9 ps (In the case of 25 Gbaud)

Calculated eye diagrams



25 Gbps NRZ



50 Gbps PAM4 (Assuming the 400GbE)

- Eye diagram calculation procedure
  - ① Approximate rational transfer function to simulated S_{dd21}
  - ② Calculate the response of the transfer function to PRBS11

  Notice : These diagrams do not contain nonlinearity and noise.

Comparison table

Reference	This work (Simulated)	[10] ISSCC '05	[13] ASSCC '05	[14] IWS '19
Technology	180 nm CMOS	180 nm BiCMOS using only MOSFETs	180 nm CMOS	180 nm CMOS
Number of cascaded stages	1	1	5	6
Core area (mm^2)	0.28	0.63	0.45	0.57
Gain (dB)	6.9	7.8	15	17
Bandwidth (GHz)	20.2	25	25.5	28
RMS jitter (ps) at 25 Gbps NRZ	0.88	N/A	N/A	1.8
Power (mW)	101	54	171	200

- Core area is 37% smaller than the previous works
- Inferior in gain and bandwidth, but superior in jitter

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Conclusion

- Differential DA is designed:
  - ① Analyze the artificial T-lines
  - ② Model the coupled inductors
  - ③ Optimize the inductors using gradient descent algorithm
- Results:
  - 37% area reduction
  - Bandwidth of 20.2 GHz
  - Nyquist group delay variation of 4.9 ps
  - Clear eye opening at 50 Gbps PAM4

→These results promote the integration of optical transceivers.

Acknowledgment

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- This presentation was supported by NEC C&C Foundation.
- This research made use of scikit-rf, an open-source Python package for RF and microwave applications.