PAPER Special Section on Microwave and Millimeter-Wave Technologies

A Compact Fully-Differential Distributed Amplifier with Coupled Inductors in 0.18-μm CMOS Technology

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SUMMARY This paper presents a compact fully-differential distributed amplifier using a coupled inductor. Differential distributed amplifiers are widely required in optical communication systems. Most of the distributed amplifiers reported in the past are single-ended or pseudo-differential topologies. In addition, the differential distributed amplifiers require many inductors, which increases the silicon cost. In this study, we use differentially coupled inductors to reduce the chip area to less than half and eliminate the difficulties in layout design. The challenge in using coupled inductors is the capacitive parasitic coupling that degrades the flatness of frequency response. To address this challenge, the odd-mode image parameters of a differential artificial transmission line are derived using a simple loss-less model. Based on the analytical results, we optimize the dimensions of the inductor with the gradient descent algorithm to achieve accurate impedance matching and phase matching. The amplifier was fabricated in 0.18-μm CMOS technology. The core area of the amplifier is 0.27 mm^2, which is 57% smaller than the previous work. Besides, we demonstrated a small group delay variation of ±2.7 ps thanks to the optimization. the amplifier successfully performed 30-Gbps NRZ and PAM4 transmissions with superior jitter performance. The proposed technique will promote the high-density integration of differential traveling wave devices.

key words: *distributed amplifier, differential amplifier, coupled inductor, CMOS integrated circuit, optimization, optical fiber communication*

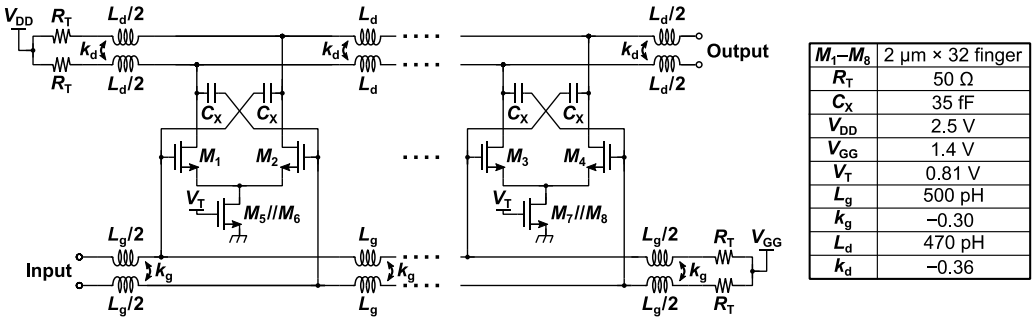
1. Introduction

The demand for information and communication technologies is increasing year by year due to the spread of cloud services. Recent communications are based on digital coherent optical transmission systems. These systems require analog circuits with high operating speeds of more than 100 Gbaud. In advanced CMOS technologies, each with a maximum oscillation frequency f_{max} of at least 200 GHz [1], a bandwidth wider than $0.25 \times f_{max}$ is required to transmit a 100-Gbaud signal. Distributed amplifiers have broad bandwidth, high output power, and excellent input-output matching. These characteristics meet the requirements. Some distributed modulator drivers reached bandwidths of nearly 100 GHz [2]–[4]. Recently, distributed drivers were also developed for quantum key transfer systems [5]. Another application of distributed amplifiers is frequency interleaving. In that case, distributed amplifiers are used for signal combining and frequency conversion [6], [7]. Distributed amplifiers are, thus, an essential component in the development of future communication technologies. On the other hand, most of the circuits used in optical transceivers have differential topology. Differential circuits have advantages in common-mode noise rejection and DC coupled cascading. Nevertheless, most of the distributed amplifiers reported in the past are single-ended [8]–[11] or pseudo-differential topologies [12]–[15]. This is because distributed amplifiers require many inductors or transmission lines to form artificial transmission lines at the input and output. In differential topology, a total of four artificial transmission lines are required, which not only consumes a large chip area but also makes layout design difficult. Although the pseudo-differential topology can simplify the layout, it does not provide the aforesaid advantages. Besides, the previous differential distributed amplifiers consume core areas of more than 0.5 mm^2 [4], [16], which raises an issue of manufacturing cost. Inductive coupling is an effective way to reduce the number and areas of inductors. For example, small-area laser drivers using coupled inductors have been reported [17], [18]. For distributed circuits, some transversal filters and mixers adopt coupled inductors [19]–[21]. In this study, we developed a small-area differential distributed amplifier using coupled inductors. We set target specifications to bandwidth $> 0.25 \times f_{max}$ and core area < 0.5 mm^2 for applying to state-of-the-art optical fiber communication systems. Figure 1 shows a schematic of the proposed amplifier. Coupled inductors reduce the area to about half that of conventional amplifiers and enable a simple layout design. A challenge to using coupled inductors is that capacitive parasitic coupling between the two inductors affects the characteristics of the lines. Undesirable capacitive coupling lowers the impedance of the artificial transmission lines and causes reflections at the termination. This not only deteriorates input-output matching but also leads to increased group delay and gain variations at low frequencies [22]. The parasitic coupling also changes the phase constant of the lines, which causes a roll-off in the gain response due to

Manuscript received November 13, 2022.
Manuscript revised March 3, 2023.
Manuscript publicized April 19, 2023.

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DOI: 10.1587/transele.2023MMP0006

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M_1–M_8	2 μm × 32 finger
R_T	50 Ω
C_X	35 fF
V_{DD}	2.5 V
V_{GG}	1.4 V
V_T	0.81 V
L_g	500 pH
k_g	−0.30
L_d	470 pH
k_d	−0.36

Fig. 1 Schematic of the proposed fully-differential distributed amplifier.

a phase mismatch between the gate and drain lines. This study derives odd-mode image parameters of the differential artificial transmission lines. The lines are optimized by a gradient descent algorithm based on the analytical solution. In recent circuit design, simulation-based optimization is widely used. Although simulation-based optimization works well when accurate device models are available, it requires significant effort for measurement and modeling. We used a simple loss-less model of the inductors extracted by electromagnetic field analysis. This reduces design time and effort, and it ensures the explainability of the circuit operation. This paper is an extended version of [23]. We added an explanation of circuit analysis with image parameters and a detailed procedure for modeling and optimization. The effectiveness of the proposed technique was demonstrated by experiments and comparison with state-of-the-art research.

2. Analysis and Design

2.1 Analysis

Figure 2 (a) shows a small signal equivalent circuit of the amplifier cell, where C_{gs}, C_{gd}, and C_{ds} are gate-source capacitance, gate-drain capacitance, and drain-source capacitance of the MOSFETs. C_X is a cross-coupled capacitor that makes the amplifier unilateral for a differential signal [24]. Assuming a differential input signal, we can consider an odd-mode half circuit shown in Fig. 2 (b). The voltage at node Z equals zero, and it can be regarded as a virtual ground. The half circuit is a paralleled connection of a hybrid-pi model of the MOSFETs and cross-coupled capacitors. The admittance matrix of the half circuit is given by

$$\boldsymbol{Y}_{\mathbf{half}} = \begin{bmatrix} j\omega(C_{gs} + C_{gd} + C_X) & j\omega(-C_{gd} + C_X) \\ g_m + j\omega(-C_{gd} + C_X) & j\omega(C_{ds} + C_{gd} + C_X) \end{bmatrix}. \tag{1}$$

When $C_X = C_{gd}$, then

$$\boldsymbol{Y}_{\mathbf{half}} = \begin{bmatrix} j\omega(C_{gs} + 2C_{gd}) & 0 \\ g_m & j\omega(C_{ds} + 2C_{gd}) \end{bmatrix}. \tag{2}$$

The amplifier becomes unilateral due to the cross-coupled capacitors. The input miller capacitance without C_X is $(1 + A_v)C_{gs}$ with a voltage gain of A_v [25], and thus, C_X decreases

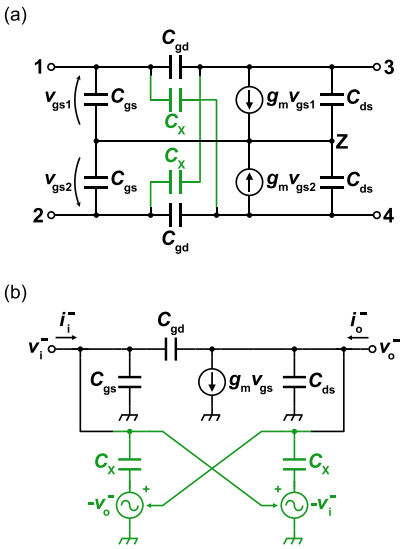


Fig. 2 Amplifier cell. (a) Small signal equivalent circuit. (b) Odd-mode half-circuit.

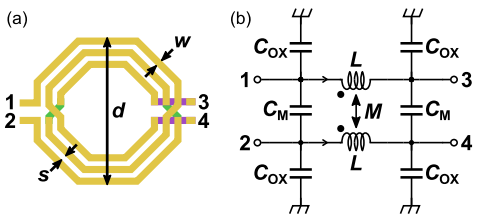


Fig. 3 Coupled inductor. (a) Layout. (b) Loss-less model.

the input capacitance when $A_v > 1$. On the other hand, the output miller capacitance is given by $(1+1/A_v)C_{gd}$, and thus, C_X slightly increases the output capacitance. However, it is almost no problem, because the bandwidth of the distributed amplifier is generally limited by the gate line, not the drain line. The important advantage of using C_X is that the drain line and gate line can be separately designed. It allows a designer to optimize the inductors as discussed later.

Figure 3 shows a layout and loss-less model of a coupled inductor. L, M, C_{OX}, and C_M are self-inductance, mutual inductance, the capacitance between the winding wire and substrate, and mutual capacitance, respectively. This loss-less model is consistent with ignoring all the parasitic resistances in the model used in [26]. The same was

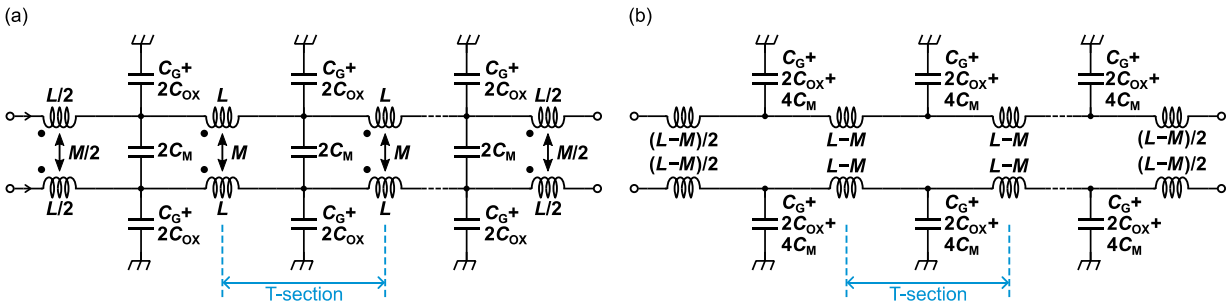


Fig. 4 (a) Circuit model of the gate line. (b) Odd-mode equivalent circuit.

also used in [27]. The sign of the mutual inductance is typically chosen to be negative so that the magnetic flux is enhanced by the differential currents. Figure 4 (a) shows an equivalent circuit of the gate line. We assumed that the input signal is in odd-mode and the amplifier cell can be regarded as a shunt capacitor $C_G = C_{gs} + 2C_{gd}$. This circuit is similar to the segmented model of a differential transmission line, and its odd-mode equivalent circuit is shown in Fig. 4 (b). This is a constant-K-type filter consisting of a series of T-sections separated by blue dashed lines. The image impedance $Z_{T,G}$ and image propagation constant $\theta_{T,G} = \alpha_{T,G} + j\beta_{T,G}$ of the T-section are given by [28]

$$Z_{T,G} = Z_G \sqrt{1 - \left(\frac{\omega}{\omega_G}\right)^2}, \tag{3}$$

$$\sinh \frac{\theta_{T,G}}{2} = j\frac{\omega}{\omega_G}, \tag{4}$$

where Z_G and ω_G represent a nominal impedance and Bragg cutoff frequency given by

$$Z_G = \sqrt{\frac{L - M}{C_G + 2C_{OX} + 4C_M}}, \tag{5}$$

$$\omega_G = \frac{2}{\sqrt{(L - M)(C_G + 2C_{OX} + 4C_M)}}. \tag{6}$$

Since $\alpha_{T,G} = 0$ holds for the pass band, $\beta_{T,G}$ is given by expanding (4) with the addition theorem as follows:

$$\beta_{T,G} = 2\sin^{-1}\frac{\omega}{\omega_G}. \tag{7}$$

Assuming $\omega \ll \omega_G$, $Z_{T,G}$ and $\beta_{T,G}$ are approximated as

$$Z_{T,G} \approx Z_G, \tag{8}$$

$$\beta_{T,G} \approx 2\frac{\omega}{\omega_G}. \tag{9}$$

The phase delay per section is given by

$$\tau_G = \frac{2}{\omega_G} = \sqrt{(L - M)(C_G + 2C_{OX} + 4C_M)}. \tag{10}$$

The same holds for the drain line by replacing C_G to C_D, and Z_D and τ_D are obtained. To minimize linear distortion, impedance and phase matching must be ensured. In other words, $Z_G = Z_D = R_T$ and $\tau_G = \tau_D$ must hold.

2.2 Modeling of the Coupled Inductor

The values of L, M, C_{OX}, and C_M vary depending on the dimensions of the coupled inductor such as a diameter d, line width w, and line space s. These relationship needs to be clarified for design optimization. The four-port Y-parameters of the inductor are obtained by

$$Y_{11} = j\left(\frac{-L}{\omega(L^2 - M^2)} + \omega(C_{OX} + C_M)\right), \tag{11}$$

$$Y_{21} = j\left(\frac{M}{\omega(L^2 - M^2)} - \omega C_M\right), \tag{12}$$

$$Y_{31} = j\left(\frac{L}{\omega(L^2 - M^2)}\right), \tag{13}$$

$$Y_{41} = j\left(\frac{-M}{\omega(L^2 - M^2)}\right), \tag{14}$$

where $Y_{11} = Y_{22} = Y_{33} = Y_{44}$, $Y_{21} = Y_{12} = Y_{43} = Y_{34}$, $Y_{31} = Y_{13} = Y_{42} = Y_{24}$, and $Y_{41} = Y_{14} = Y_{32} = Y_{23}$ hold due to symmetry. Solving the simultaneous equations from (11) to (14) gives

$$L = \frac{\mathrm{Im}(Y_{31})}{\omega\,\mathrm{Im}(Y_{31})^2 - \omega\,\mathrm{Im}(Y_{41})^2}, \tag{15}$$

$$M = \frac{-\mathrm{Im}(Y_{41})}{\omega\,\mathrm{Im}(Y_{31})^2 - \omega\,\mathrm{Im}(Y_{41})^2}, \tag{16}$$

$$C_{OX} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{31}) + \mathrm{Im}(Y_{41}) + \mathrm{Im}(Y_{21})}{\omega}, \tag{17}$$

$$C_M = \frac{-\mathrm{Im}(Y_{41}) - \mathrm{Im}(Y_{21})}{\omega}. \tag{18}$$

Thus, the values of L, M, C_{OX}, and C_M can be extracted from four-port Y-parameters that are obtained by electromagnetic analysis or measurement. In the following, a modeling procedure is explained with self-inductance as a representative, and the same holds for $M(d, s, w)$, $C_{OX}(d, s, w)$, and $C_M(d, s, w)$. The model formula for self-inductance is defined as a following quadratic polynomial.

$$L(d, s, w) \equiv \alpha_0 d^2 + \alpha_1 s^2 + \alpha_2 w^2 + \alpha_3 ds + \alpha_4 dw + \alpha_5 sw + \alpha_6 d + \alpha_7 s + \alpha_8 w + \alpha_9, \tag{19}$$

where α_i ($i \in \mathbb{N}$, $i < 10$) are coefficients to be determined. We analyzed various inductors listed in Table 1

Table 1 Dimensions of the inductors for modeling.

Dimensions	Values
d (μm)	90, 110, 130, 150
s (μm)	2, 5, 7, 10
w (μm)	2, 4, 6
Number of turns	2.5 (Both primary and secondary turns)

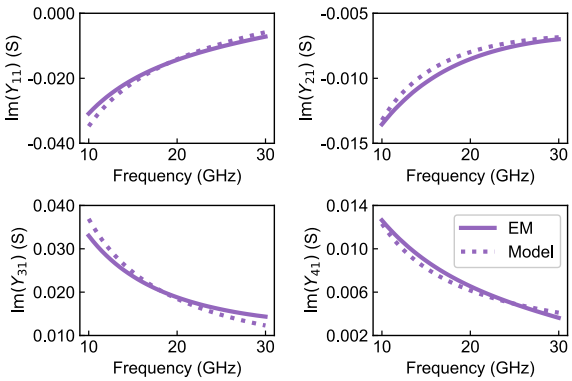


Fig. 5 Fitting result of the scalable modeling at $d = 120\ \mu$m, $s = 6\ \mu$m, and $w = 5\ \mu$m.

with Keysight's Momentum electromagnetic simulator, and a vector of the self-inductance was obtained as follows.

$$\boldsymbol{L} = \begin{bmatrix} L_1(d_1, s_1, w_1) \\ L_2(d_2, s_2, w_2) \\ \vdots \\ L_{\mathrm{N}}(d_{\mathrm{N}}, s_{\mathrm{N}}, w_{\mathrm{N}}) \end{bmatrix}, \tag{20}$$

where N is the number of inductors. The model parameters minimizing the squared error between the model and extracted values can be determined by [29]

$$[\hat{\alpha}_0 \quad \hat{\alpha}_1 \quad \cdots \quad \hat{\alpha}_9]^T = (\boldsymbol{D}^T\boldsymbol{D})^{-1}\boldsymbol{D}^T\boldsymbol{L}, \tag{21}$$

where $\boldsymbol{D}$ is a matrix of the dimensions defined as

$$\boldsymbol{D} \equiv \begin{bmatrix} d_1^2 & s_1^2 & w_1^2 & d_1 s_1 & \cdots & w_1 & 1 \\ d_2^2 & s_2^2 & w_2^2 & d_2 s_2 & \cdots & w_2 & 1 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ d_{\mathrm{N}}^2 & s_{\mathrm{N}}^2 & w_{\mathrm{N}}^2 & d_{\mathrm{N}} s_{\mathrm{N}} & \cdots & w_{\mathrm{N}} & 1 \end{bmatrix}. \tag{22}$$

The fitted model formula $\hat{L}(d, s, w)$ is obtained by substituting the model parameters $\hat{\alpha}_i$ into (19). Figure 5 shows a modeling result at $d = 120\ \mu$m, $s = 6\ \mu$m, and $w = 5\ \mu$m. This dimension was not used for modeling. The broken lines and solid lines represent Y-parameters obtained from the electromagnetic analysis (EM) and model. The model agreed well with the EM from 10 GHz to 30 GHz.

2.3 Optimization

Impedance and phase matching must be ensured to design a differential distributed amplifier with superior performance. The goal of the optimization is to find dimensions that satisfy the impedance and phase matching conditions. Since these conditions are primarily determined by the imaginary part of the impedance, the use of a loss-less model is appropriate. The mismatch between the nominal impedance and terminating resistance causes reflection waves. These reflections degrade not only input and output matching but also the flatness of frequency response of gain and group delay [22]. That is to say, the following equation needs to be satisfied.

$$\min|Z_{\mathrm{G}} - R_{\mathrm{T}}| \cap \min|Z_{\mathrm{D}} - R_{\mathrm{T}}|, \tag{23}$$

On the other hand, a mismatch between τ_{G} and τ_{D} causes a roll-off like a transversal filter. The delay matching is corresponded to the cutoff matching by considering (10). Thus, the following equation needs to be satisfied.

$$\min|\tau_{\mathrm{G}} - \tau_{\mathrm{D}}| \Leftrightarrow \min|\omega_{\mathrm{G}} - \omega_{\mathrm{D}}|. \tag{24}$$

The other requirement is maximizing the cutoff frequency. The artificial transmission lines have a significantly large peak in group delay response near the cutoff frequency, which degrades the signal quality. The cutoff frequency is limited by the gate line because C_{G} is typically larger than C_{D}. This requirement is given by

$$\max \omega_{\mathrm{G}}. \tag{25}$$

The image impedance and cutoff frequency are determined by the dimensions of the inductors. The design of the inductors is a multi-objective and multi-variable optimization problem, and it is difficult to find the optimum dimensions by repeating the electromagnetic analysis. In this research, we determined the dimensions by numerical optimization based on the analytical solutions. We defined an evaluation function for the gate line as follows.

$$E_{\mathrm{G}}(d, s, w) = \zeta_0(Z_{\mathrm{G}} - R_{\mathrm{T}})^2 + \zeta_1(-\omega_{\mathrm{G}}), \tag{26}$$

where ζ_0 and ζ_1 are weighting factors that are positive constants. Z_{g} and ω_{g} are given by (5) and (6), and L, M, C_{OX}, and C_{M} are functions of d, s, and w as described in (19). E_{G} is, therefore, a function of d, s, and w. This captures the trade-off between L, M, C_{OX}, and C_{M}. The optimum dimensions of the gate inductors can be fined by minimizing E_{G}. It satisfies the impedance matching condition and maximizes the cutoff frequency. Similarly, the evaluation function for the drain line was defined as follow.

$$E_{\mathrm{D}}(d, s, w) = \eta_0(Z_{\mathrm{D}} - R_{\mathrm{T}})^2 + \eta_1(\omega_{\mathrm{G}} - \omega_{\mathrm{D}})^2, \tag{27}$$

where η_0 and η_1 are weighting factors. The first term and second term represent the requirements for impedance matching and phase matching. The dimensions of the drain line inductors are also determined by minimizing E_{D}.

The optimum point was searched using the gradient descent algorithm [30]. The ranges of the dimensions were constrained in $90\ \mu\mathrm{m} \le d \le 150\ \mu\mathrm{m}$, $2\ \mu\mathrm{m} \le s \le 10\ \mu\mathrm{m}$ and $4\ \mu\mathrm{m} \le w \le 8\ \mu\mathrm{m}$ so that the quality factor of the inductors would not become too small. The number of steps

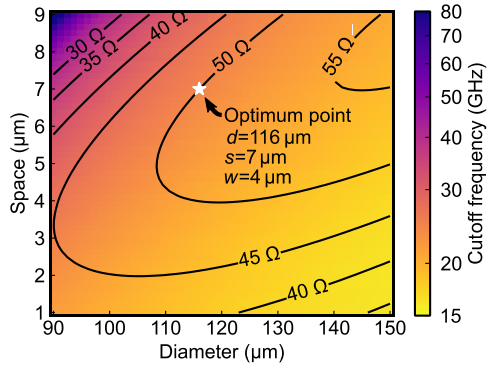


Fig. 6 Optimization result of the gate line. The solid lines and gradation represent Z_G and f_G at $w = 4$ μm, respectively.

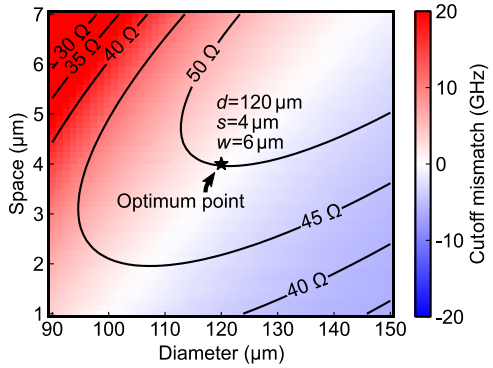


Fig. 7 Optimization result of the drain line. The solid lines and gradation represent Z_D and $(f_D - f_G)$ at $w = 6$ μm, respectively.

was 10000, and the dimensions were randomly changed every 100 steps to prevent convergence to the local optimum solutions. Figure 6 shows an optimization result for the gate line, where the solid lines and gradation represent Z_G and $f_G = \omega_G/2\pi$, respectively. The optimization converged to a point where $d = 116$ μm, $s = 7$ μm, and $w = 4$ μm. Z_G and f_G converged 50.0 Ω and 24.5 GHz at the optimum point. The f_G was maximized on the 50-Ω contour line, which satisfied impedance matching and maximized the cutoff frequency. Figure 7 shows an optimization result for the drain line. The dimensions converged to $d = 120$ μm, $s = 4$ μm, and $w = 6$ μm. Z_D and $f_D = \omega_D/2\pi$ were 50.1 Ω and 24.9 GHz at the optimum point. The error between f_G and f_D was only 2%, which satisfied the phase matching condition. This error was mainly caused by rounding the dimensions to the integer. The optimization took only 4.14 seconds on an author's laptop.

2.4 Prototyping

The amplifier was fabricated in Rohm's one-poly five-metal 0.18-μm standard CMOS process. The measured f_{max} of the n-MOSFET was 65 GHz [31]. The top and bottom metal layers were used for the inductor winding and ground wiring, respectively. The bottom metal under the inductors was removed, and the silicon substrate was exposed. A higher resistance silicide block area was specified on the exposed silicon substrate to prevent eddy current losses. The number of turns of the edge inductors was set to one and their diameters were varied to be close to $L_g/2$ and $L_d/2$ while maintaining the width and spacing. The self-inductances of the gate and drain edge inductors were 270 pH and 250 pH at 20 GHz, respectively. C_X was implemented with metal-insulator-metal capacitors, and R_T was implemented with poly resistors. The poly resistors were placed on a thick insulator for shallow trench isolation, which provided a small parasitic capacitance of 4.8 fF. Figure 8 shows a micrograph of the fabricated chip. The coupled inductors reduced the complexity of wiring. The core area was 0.35 mm × 0.76 mm = 0.27 mm^2, and the whole chip area including all the test pads was 1.1 mm × 0.66 mm = 0.73 mm^2. The bias voltages were $V_{DD} = 2.5$ V and $V_{GG} = 1.4$ V. The value of V_T was adjusted so that the tail current of each stage was 7.5 mA in both simulation and measurement. The amplifier drew a current of 30 mA and consumed a power of 75 mW.

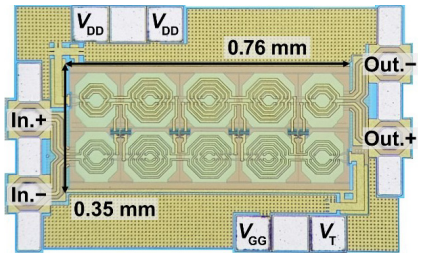


Fig. 8 Micrograph of the fabricated chip.

3. Measurement and Discussion

The four-port S-parameters were measured using Keysight's PNA-X N5247A vector network analyzer. The measurement frequency range was 0.1 GHz to 30 GHz with a frequency step of 0.1 GHz. Figure 9 (a) shows the differential gain and input and output reflection coefficients. The gain at 0.1 GHz was 5.1 dB and the 3-dB bandwidth was 18.5 GHz. The measurement results agree well with the slow-corner post-layout simulation results. Assuming a 30-Gbaud signal, the gain variation was ±1.1 dB below the Nyquist frequency of 15 GHz. The gain variation was mainly due to the propagation losses of the artificial transmission lines. A steep roll-off was observed at 25 GHz. This was consistent with the theoretical cutoff frequency of the artificial transmission lines. The input and output reflections of S_{dd11} and S_{dd22} were less than −15 dB and −13 dB, respectively. A small impedance mismatch was achieved by the optimization. Figure 9 (b) shows common-mode gain and isolation. The common-mode gain was nearly −10 dB that is smaller than the differential gain thanks to the fully-differential topology. S_{dd12} was smaller than −20dB because the amplifier cell was unilateralized by C_X. Figure 9 (c) shows group delay responses. To eliminate the variation due to the measurement noise, a moving average of 10 nearby

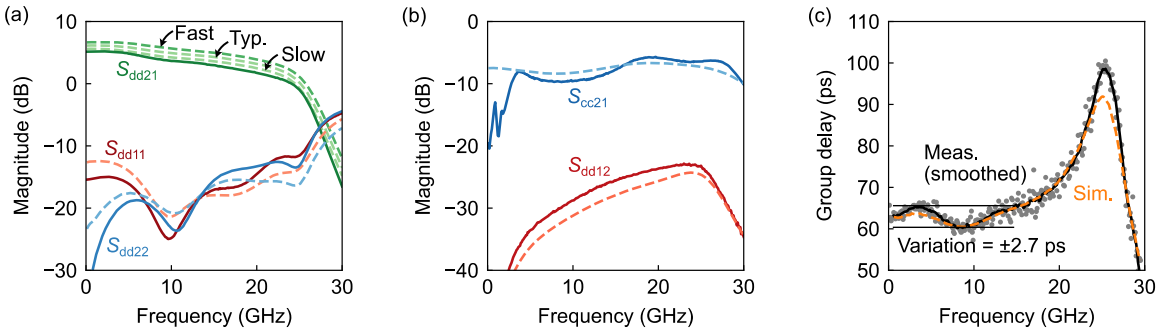


Fig. 9 Measured S-parameters. The solid lines and dashed lines represent the measurement and simulation. Unless otherwise indicated, the simulation results are slow corner. (a) Differential gain and reflection. (b) Common-mode gain and in-out isolation. (c) Group delay response.

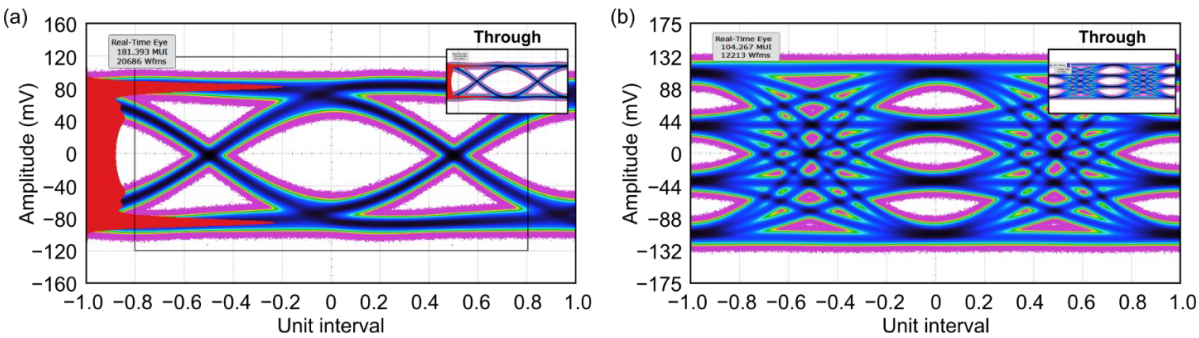


Fig. 10 Measured eye diagram. (a) 30-Gbps NRZ. (b) 30-Gbps PAM4. Inset: eye diagram with a through structure.

points is shown as a solid line. We demonstrated a small group delay variation of ±2.7 ps below the Nyquist frequency. This flat group delay response indicates that the impedance and phase matching of the artificial transmission lines is properly ensured. Then, we performed a time domain measurement. Keysight's M8195A arbitrary generator and UXR1104A real-time oscilloscope were connected to the input and output of the amplifier. The input signal was a differential pseudo-random signal with a length of $2^9 - 1$. The differential outputs were connected to Ch.1 and Ch.3 of the oscilloscope, and the Ch.3 signal was observed. The linear distortion due to the RF cables and probes was removed by the channel de-embedding before the measurement. Figure 10 (a) shows an eye diagram for a 30-Gbps NRZ signal. The inset shows the through measurement with a calibration standard. The output swing was 100 mV_{PP} and 160 mV_{PP} for the through and amplifier. The estimated timing margin at a bit error rate of 10^{-12} for the thorough and amplifier was 0.88UI and 0.75UI, and the root-mean-square jitter was 0.34 ps and 0.42 ps, respectively. The optimization reduced the group delay variation, resulting in small jitter degradation. Figure 10 (b) shows an eye diagram for a 30-Gbps PAM4 signal. The output swing was 130 mV_{PP} and 220 mV_{PP}. The eye width was 0.5UI and 0.4UI for the through and amplifier, achieving 30-Gbps PAM4 transmission.

Table 2 lists a performance summary and comparison with the distributed amplifiers previously reported. Rito et al. [4] reported a distributed modulator driver using SiGe:C BiCMOS technology with f_{max} = 500 GHz. Taking advantage of the excellent device performance, 90-Gbps PAM4 transmission was demonstrated. However, the bandwidth normalized by f_{max} is 0.18, which is not a particularly wide bandwidth from the point of view of the circuit. Wu et al. [8] introduced a frequency interleaving technique and reported excellent bandwidth. However, this technique causes rapid group delay variations at the sub-band junctions. Lee et al. [9] proposed a distributed amplifier using deeply doped channel technology, which has very low power consumption. The amplifiers reported in [12]–[15] used a pseudo-differential topology. Pseudo-differential does not provide the advantages of differential circuits. The distributed amplifier reported in this study has a small core area of 0.27 mm^2 and a fully-differential topology. Compared to the most similar circuit [16], the coupled inductors allow a 57% reduction in silicon area. Although [5]–[9] used the single-ended topology, they have a larger core area than this work. The developed amplifier has a small power consumption of 75 mW at the cost of the gain. The gain can be increased by cascading amplifiers [8]. A future challenge is to develop a high-gain distributed amplifier that takes advantage of the fully-differential topology that allows true DC coupled cascading. The bandwidth normalized by f_{max} was 0.28, achieving the target specification. By applying the proposed circuit to advanced processes with f_{max} > 200 GHz,

Table 2 Performance comparison with the previous distributed amplifiers.

Reference	Technology	Topology	Core area[†] (mm^2)	BW[††] (GHz) (BW / f_{max})	Gain (dB)	OP_{1dB} (dBm)	GDV[†††] (ps)	Datarate[‡] (Gbps)	Jitter[‡‡] (ps)	Power (mW)
This work	0.18-µm CMOS	Fully-diff.	0.27	DC−18.5 (0.28)	5.1	3.7[‡‡‡] (sim.)	±2.7 (< 15 GHz)	30/30	0.42	75
[3] T.MTT '17	0.13-µm BiCMOS	Fully-diff.	0.56	DC−90 (0.18)	12.5	13.5[‡‡‡]	±5 (< 67 GHz)	120/90	0.6	550
[4] T.VLSI '22	0.25-µm CMOS	Single-ended	1.68	DC−12 (N.R.)	11.54	10−18	±100 (< 10 GHz)	N.R./N.R.	N.R.	666
[7] T.VLSI '22	65-nm CMOS	Single-ended	0.57	2−68 (N.R.)	17.2	−1	±10 (10−60 GHz)	N.R./N.R.	N.R.	120
[8] TR EL '22	55-nm DDC[*] CMOS	Single-ended	0.54	DC−29 (N.R.)	5.95	−11 (sim.)	N.R.	N.R./N.R.	N.R.	5.32
[11] ASSCC '21	65-nm CMOS	Pseudo-diff.	0.77[**]	3−78 (N.R.)	16.9	7.45[‡‡‡]	±18 (5−75 GHz)	N.R./N.R.	N.R.	151
[12] IMS '19	65-nm CMOS	Pseudo-diff.	1.0	DC−34 (N.R.)	15	N.R.	N.R.	64/N.R.	N.R.	960
[13] MWCL '18	90-nm CMOS	Pseudo-diff.	0.58	DC−28.2 (N.R.)	17	N.R.	N.R.	40/N.R.	N.R.	650
[14] T.MTT '12	65-nm LP[***] CMOS	Pseudo-diff.	0.94[**]	DC−65 (0.33)	22	10[‡‡‡]	±20 (< 65 GHz)	N.R./N.R.	N.R.	97
[15] ISSCC '05	0.18-µm BiCMOS[****]	Fully-diff.	0.63	DC−25 (N.R.)	7.8	2.6[‡‡‡]	N.R.	N.R./N.R.	N.R.	54

[†]Estimated from the micrographs. [††]Bandwidth. [†††]Group delay variation. [‡]NRZ/PAM4. [‡‡]Root-mean-square jitter. [‡‡‡]Differential. [*]Deeply depleted channel. [**]Including an input distributed active balun. [***]Low power. [****]Using only MOSFETs.

a bandwidth of 56 GHz or higher is expected and enables 100 Gbaud transmissions. In addition, loss compensation can be used to further extend the bandwidth reached to the theoretical bandwidth of 25 GHz. Besides, PAM4 transmission was demonstrated only in this study and [4]. These studies reported small group delay variations of less than ±5 ps. Therefore, it is important to strictly satisfy the impedance and phase matching conditions for multi-level transmission.

4. Conclusion

We presented a compact fully-differential distributed amplifier that reduces a silicon area by more than 50%. To achieve a flat frequency response, we analyzed the differential artificial transmission lines using a simple loss-less model. The lines were optimized by a gradient descent algorithm based on the derived odd-mode image parameters. The phase and impedance matching were strictly satisfied by the optimization, and we demonstrated a small group delay variation of ±2.7 ps and 30-Gbps NRZ and PAM4 transmission. Therefore, these results will accelerate the high-density integration of differential distributed circuits.

Acknowledgments

This work was supported through the activities of VDEC, The University of Tokyo, in collaboration with Rohm Corporation, Toppan Printing Corporation, Cadence Design Systems, Mentor Graphics, and Keysight Technologies.

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