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# Bandwidth Tripler: Broadband Signal Generation with an Image-Rejection Analog Multiplexer for Fiber Optic Transmitters

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***Abstract*— This paper describes a frequency-interleaved digital-to-analog conversion technique named bandwidth tripler with an image-rejection analog multiplexer (AMUX). The tripler extends the bandwidth of the parallelized sub-DACs by three times in the frequency domain. Image rejection using the phase-shifted method reduces analog filters for combining divided sub-bands, which improves the signal quality and size of the analog circuits. Besides, the tripler outputs no spurious signals out of the target bandwidth. The AMUX for the tripler was fabricated in 180-nm CMOS technology. Pseudo-differential switches were used to reduce distortion, and a broadband termination circuit was inserted at the output of the AMUX to compensate for the limited performance of the CMOS devices. The fabricated AMUX was evaluated by S-parameter and time-domain measurements. The S-parameter measurement results demonstrated a bandwidth of 23.4 GHz. In addition, broadband signal generation for 30 Gbps PAM4 was demonstrated without using any equalization. The power consumption of the AMUX was only 49 mW. This high-speed performance is comparable to the conventional DACs fabricated using advanced CMOS processes.**

***Index Terms*—Analog multiplexer (AMUX), CMOS, digital-to-analog converter (DAC), fiber-optic communication, integrated circuit, interleaved DAC, optical transmitter.**

## I. Introduction

DEMAND for fiber optic communications has been increasing due to the growth of cloud services, mobile communications, and streaming media. The data rates of Ethernet optical transceivers have already reached 400 Gbps, and the next generations of 800 Gbps and 1.6 Tbps will be commercially available in the near future [1]-[2]. To improve the data rates, dense wavelength division multiplexing is used, however, increasing the number of multiplexes degrades the costs due to the many optical transceivers. To achieve high capacity without increasing costs, the baud rate of optical transceivers needs to be extended. Fig. 1 shows a typical configuration of an optical transmitter. The transmitter consists of a laser diode (LD), digital signal processor (DSP), digital-to-analog converters (DACs), Mach–Zehnder modulators (MZMs), and their drivers. The DSP shapes waveform to compensate for the linear and non-linear distortions of the optic devices and codes for error correction. The DACs convert the digital signals from the DSP into analog signals. The DACs output pulse amplitude modulation (PAM) signals, and the optical modulators output quadrature amplitude modulation (QAM) signals. The DACs are usually fabricated using CMOS technology to integrate with the DSP [3]-[7]. Continuous engineering efforts have been made to increase the speed of CMOS DACs. Most CMOS DACs for optical transmitters are based on current-mode logic (CML) architecture also known as current steering DACs. The bandwidth of the CML-based DAC using a 7-nm FinFET process reaches 40 GHz [3]. However, the maximum oscillation frequency, $f_{\max}$ , of FinFETs decreases with process shrink [8], making further bandwidth extension difficult. To overcome this difficulty, several DAC interleaving concepts have been investigated, which parallelize multiple DACs. One of the simplest DAC interleaving concepts is time interleaving [7], [9]-[13]. In this concept, multiple DACs are driven by clocks in different phases, and their outputs are combined with an analog combiner [7], [9] or analog multiplexer (AMUX) [10]-[13]. The combiner increases the sample rate by the number of parallelized DACs, but bandwidth remains the same as before interleaving. In construct, the AMUX, an analog selector circuit, improves not only the sample rate but also the bandwidth thanks to the non-linear switching operation. [10] demonstrated 100-Gbaud signal generation with an AMUX fabricated in SiGe BiCMOS technology.

The other alternative methods are frequency interleaving that also improves the bandwidth [14]-[19]. In these methods, the spectrum of the target signal is divided by digital signal

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preprocessing using fast Fourier transform (FFT). The divided signals are frequency-converted and combined with analog circuits. The digital band interleaving (DBI) method uses single-sideband mixers for up-conversion [16]. The divided bands are combined with a triplexer composed of analog filters and combiners that are implemented on printed circuit boards [20], [21]. Three-times bandwidth extension has been demonstrated with the DBI method, but the triplexers degrade manufacturing costs, footprints, and signal quality. To compensate for the frequency response degraded by the triplexer, which requires complex digital equalization. The bandwidth doubler is a solution to this problem [17]-[19], which generates broadband signals by digital signal preprocessing and a 2:1 AMUX. [17] demonstrated 168-Gbaud signal generation with a 110-GHz-bandwidth AMUX fabricated in an InP double heterojunction bipolar transistor (DHBT) technology. However, the number of multiplexing is as small as 2:1, which requires a higher bandwidth for the parallelized sub-DACs.

Our group has therefore proposed a bandwidth tripler that extends the bandwidth by three times with an image-rejection AMUX [22]. The tripler does not require analog filters and complex equalization. We have also developed an image-rejection AMUX for the tripler in CMOS technology [23]. The CMOS-based AMUX has the possibility of reducing power consumption, footprints, and manufacturing costs by monolithic or hybrid integration with digital circuits, sub-DACs, and silicon photonics devices. However, the bandwidth extension with an image-rejection AMUX has been reported only by simulation, and no experimental results have been reported. This paper reports the first experimental demonstration of the bandwidth tripler with an image-rejection AMUX. This is an extended paper based on [23]. We provide a mathematical description of the bandwidth tripler, S-parameter and time-domain measurement results, a comparison with the cutting-edge CMOS DACs, and discussions on the challenges identified through the measurement. This paper is organized as follows. Section II describes the principle of the tripler; Section III presents the design of the CMOS image-rejection AMUX; Section IV provides the results of the experiments and performance comparison with cutting-edge AMUXs and CMOS DACs; Section V concludes this paper.

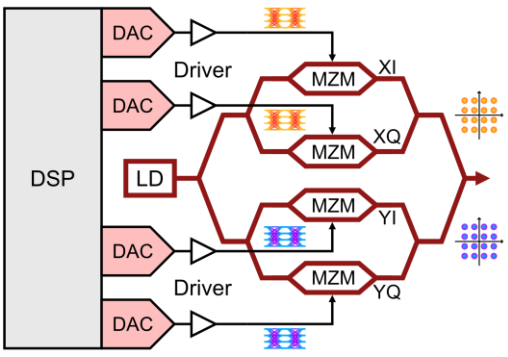
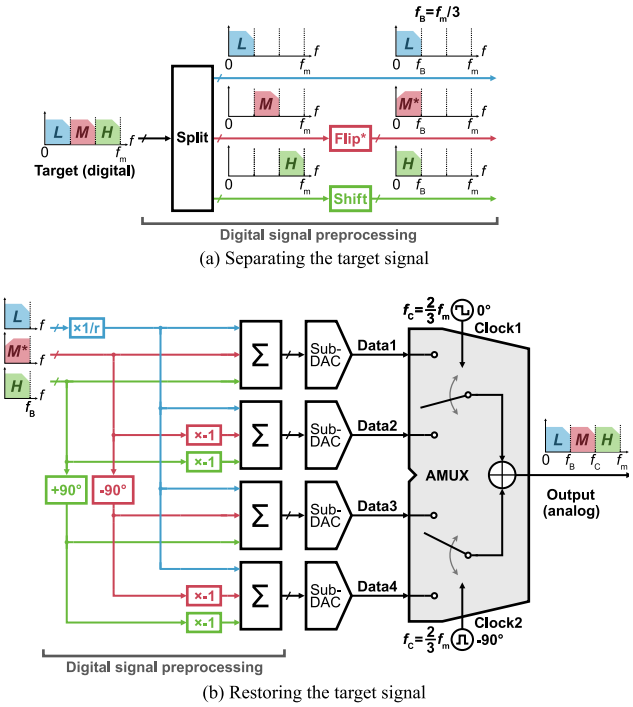



Fig. 1 Optical transmitters for digital coherent systems.




(a) Separating the target signal

(b) Restoring the target signal

Fig. 2 Block diagram of the bandwidth tripler.

## II. Bandwidth Tripler

The bandwidth tripler was first reported in [22]. In this paper, we describe the principle of the tripler mathematically. Fig. 2 shows a block diagram of the bandwidth tripler. The tripler is composed of a digital signal processor, four sub-DACs, and an AMUX. First, the bandwidth of the target signal is limited by a roll-off filter with a bandwidth of $f_{\mathrm{m}}$. The target signal is transformed into the frequency domain by FFT and separated into three sub-bands: low-band $L(f)+L^*(-f)$, mid-band $M(f)+M^*(-f)$, and high-band $H(f)+H^*(-f)$. The bandwidth of each sub-band is $f_{\mathrm{B}}=f_{\mathrm{m}}/3$. The target signal spectrum is given by the summation of the separated sub-bands similarly to [17] as follows:

$$S_{\mathrm{target}}(f)=L(f)+M(f)+H(f)+L^*(-f)+M^*(-f)+H^*(-f), \quad (1)$$

where the asterisks represent complex conjugate, and the range of variable $f$ is $[-f_{\mathrm{m}}, f_{\mathrm{m}}]$. Unlike [17], the negative frequency components are expressed here to show the Hermite symmetry. Although only the positive frequency components are illustrated in Fig. 2, all spectrums satisfy Hermite symmetry. Next, the mid-band and high-band are shifted to the baseband, and the mid-band is flipped and conjugated. As a result of the above operations, each sub-band is placed within $f_{\mathrm{m}}/3$ that is the bandwidth of the sub-DACs as shown in Fig. 2(a). Then, the separated sub-bands are restored by multiplying the clock signals using an analog multiplexer (AMUX) as shown in Fig. 2(b). The clock frequency is $f_{\mathrm{C}}=2f_{\mathrm{m}}/3$. To avoid degrading the signal quality and increasing the manufacturing costs, the bandwidth tripler uses image rejection by the phase-shifted method. Fig. 3(a) shows the mathematical model of image

rejection for the mid-band. The data3 and data4 are −90° out of phase with the data1 and data2, respectively. The clock2 is also −90° out of phase with the clock1. The bandwidth tripler operates as a single sideband (SSB) mixer that outputs the lower sideband (LSB) for the mid-band. The −90° phase shifter is a Hilbert transformer, and the frequency response is given by

$$\sigma_{\mathrm{M}}(f)=\begin{cases}-j=e^{-j\pi/2}, & \text{for } f>0\\ 0, & \text{for } f=0\\ +j=e^{+j\pi/2}, & \text{for } f<0\end{cases} \quad (2)$$

The spectrums at nodes α and β are given by

$$S_{\alpha}(f)=M(f+f_{\mathrm{C}})+M^{*}(-f+f_{\mathrm{C}}) \quad (3)$$

$$S_{\beta}(f)=jM(f+f_{\mathrm{C}})-jM^{*}(-f+f_{\mathrm{C}}) \quad (4)$$

Focusing on the fundamental frequency of the clock signals, the clock1 and clock2 are given by

$$s_{\mathrm{clk1}}(t)=\cos 2\pi f_{\mathrm{C}}t=\frac{e^{j2\pi f_{\mathrm{C}}t}+e^{-j2\pi f_{\mathrm{C}}t}}{2}, \quad (5)$$

$$s_{\mathrm{clk2}}(t)=\sin 2\pi f_{\mathrm{C}}t=\frac{e^{j2\pi f_{\mathrm{C}}t}-e^{-j2\pi f_{\mathrm{C}}t}}{2j}. \quad (6)$$

The spectrums at node γ and δ are given by

$$S_{\gamma}(f)=\frac{1}{2}[M(f)+M(f+2f_{\mathrm{C}})]+\frac{1}{2}[M^{*}(-f+2f_{\mathrm{C}})+M^{*}(-f)], \quad (7)$$

$$S_{\delta}(f)=\frac{1}{2}[-j\cdot jM(f)+j\cdot jM(f+2f_{\mathrm{C}})]+\frac{1}{2}[-j\cdot -jM^{*}(-f+2f_{\mathrm{C}})+j\cdot -jM^{*}(-f)]. \quad (8)$$

Therefore, the image signal at the upper sideband (USB) is rejected by adding $S_{\gamma}(f)$ and $S_{\delta}(f)$, and the mid-band is placed in the target frequency as follows:

$$S_{\epsilon}=S_{\gamma}(f)+S_{\delta}(f)=M(f)+M^{*}(-f). \quad (9)$$

Fig. 3(b) shows the mathematical model for the high-band. It is the same as the mid-band, except that the phase shifter is +90°. The spectrums at node ζ and η are given by

$$S_{\zeta}(f)=H(f+f_{\mathrm{C}})+H^{*}(-f+f_{\mathrm{C}}), \quad (10)$$

$$S_{\eta}(f)=jH(f+f_{\mathrm{C}})-jH^{*}(-f+f_{\mathrm{C}}). \quad (11)$$

Note that the positive and negative frequency components are in opposite directions for the mid- high-bands. $S_{\zeta}(f)$ and $S_{\eta}(f)$ is up-converted by multiplying by the clock signals. The spectrums at node θ and κ are given by

$$S_{\theta}(f)=\frac{1}{2}[H(f)+H(f+2f_{\mathrm{C}})]+\frac{1}{2}[H^{*}(-f+2f_{\mathrm{C}})+H^{*}(-f)], \quad (12)$$

$$S_{\kappa}(f)=\frac{1}{2}[-j\cdot jH(f)+j\cdot jH(f+2f_{\mathrm{C}})]+\frac{1}{2}[-j\cdot -jH^{*}(-f+2f_{\mathrm{C}})+j\cdot -jH^{*}(-f)]. \quad (13)$$

The LSB is rejected by adding $S_{\theta}(f)$ and $S_{\kappa}(f)$, and the high-band is also placed in the target frequency as follows:

$$S_{\lambda}=S_{\theta}(f)+S_{\kappa}(f)=H(f)+H^{*}(-f). \quad (14)$$

Fig. 3(c) shows the mathematical model for the low-band. The low-band is not multiplied by the clock signals because all data signals are the same for the low-band. Thus, the low-band passes through the tripler. The spectrum at node $\xi$ is given by

$$S_{\xi}=\frac{2}{r}[L(f)+L^{*}(-f)]. \quad (15)$$

The amplitude of the low-band is previously multiplied by $1/r$ to align the amplitude with the mid- and high-bands. In the mathematical model, the amplitude of each sub-band is aligned when $r=2$. However, the up-conversion gain of the AMUX is smaller than the gain for the through output in experiments, which causes amplitude unbalances. The experimental value of $r$ is determined by outputting sinusoidal pilot signals from the AMUX. Finally, adding the divided sub-bands before digital-to-analog conversion, the output of the AMUX agrees with the target signal as follows:

$$S_{\epsilon}(f)+S_{\lambda}(f)+S_{\xi}(f)=S_{\mathrm{target}}(f). \quad (16)$$

Since each sub-band is combined in the digital domain, not the analog domain, the timing between the sub-bands is perfectly aligned without calibration, which improves the signal quality.

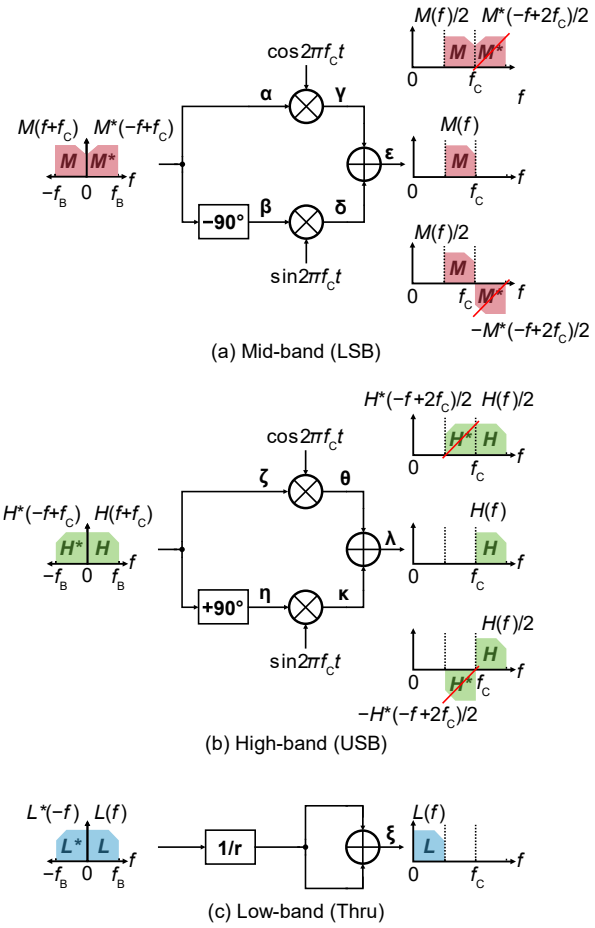
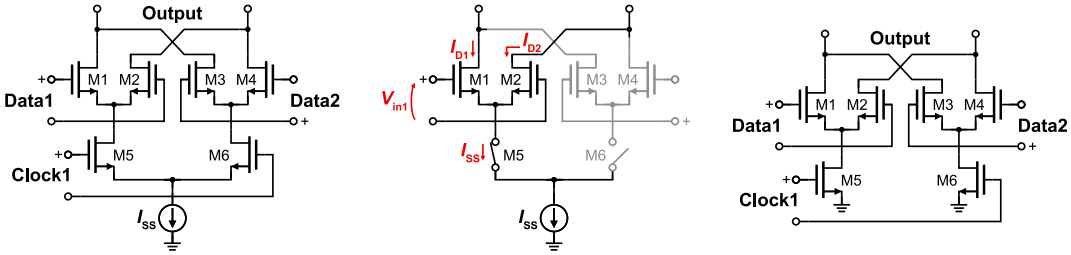



Fig. 3 Mathematical model of the bandwidth tripler.

## III. AMUX

The bandwidth tripler requires an image-rejection AMUX. The image-rejection AMUX is composed of two exclusive switches and a combiner. The tripler requires ultra-fast switching operations because the AMUX determines the bandwidth of the transmitter. To cope with this requirement, we




(a) Schematic of the exclusive switch (b) Simplified model (c) Pseude differential switch

Fig. 4 Gilbert cell-based switches.

used Gilbert cell-based switches. They are suitable for the AMUX because they have a fast-switching characteristic compared with other switching schemes such as transmission gates. However, the nonlinearity and limited $f_{max}$ of the MOSFETs in CMOS technology degrade the performance of the AMUX. Most conventional AMUXs are fabricated using bipolar transistors, which offer superior linearity and operation speed [17], [24]. On the other hand, CMOS AMUXs have the potential to reduce assembly costs, footprints, connection losses, and power consumption by monolithic or hybrid integration with the sub-DACs and silicon photonic devices. These advantages more than make up for the lower performance of MOSFETs. This chapter describes a design of a CMOS image-rejection AMUX. Sections III-A and III-B discuss the linearity and bandwidth, respectively.

### *A. Gilbert Cell-Based Switches*

Fig. 4(a) shows the schematic of the Gilbert cell-based switch. The upper differential pairs are driven by small-amplitude data signals and operate linearly. The lower differential pairs are driven by large-amplitude clock signals and operate like switches. All transistors are biased in the saturation region to prevent spurious signals caused by the distortions. Most of the Gilbert cell mixers for wireless communications have large-amplitude local oscillator input at the upper differential pairs and small-amplitude radio frequency input at the lower differential pairs. Thus, the upper and lower sides are reversed in the image-rejection AMUX, which reduces the number of differential pairs. The disadvantage of Gilbert cell-based switches using a CMOS process is nonlinearity, which is a contrast to the excellent linearity of the bipolar transistors. The distortions caused by the nonlinearity degrade the signal quality. To improve the linearity of CMOS Gilbert cells, the bias currents of the data input MOSFETs need to be increased. A well-known linearization technique is current bleeding (charge injection) [25], [26], but it can be used only when the lower side is the small-signal input.

To analyze the distortions caused by the data input MOSFETs, we consider a simplified Gilbert cell-based switch as shown in Fig. 4(b). The clock input MOSFETs are approximated as ideal switches. When the left-side switch is on-state, the output current is given by

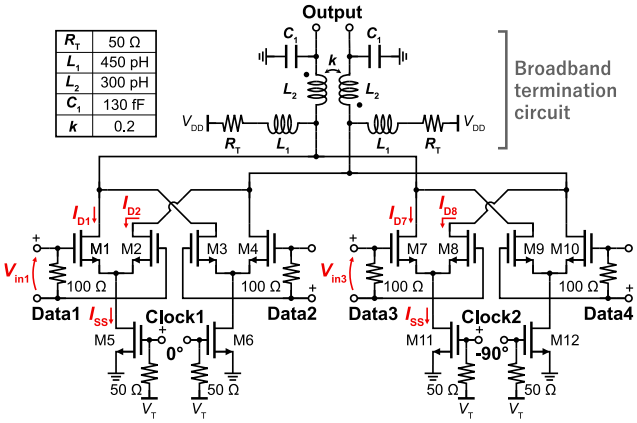



Fig. 5 Schematic of the image-rejection AMUX.

$$I_{D1} - I_{D2} = \frac{\beta}{2} V_{in1} \sqrt{\frac{4I_{SS}}{\beta} - V_{in1}^2}, \quad [27] \qquad (17)$$

where $\beta$ represent a gain coefficient of the MOSFETs. Assuming $V_{in1} \ll 1$, (17) is approximated as follows:

$$I_{D1} - I_{D2} \approx \sqrt{\beta I_{SS}} V_{in1} - \frac{\beta}{8} \sqrt{\frac{\beta}{I_{SS}}} V_{in1}^3 \equiv G_1 V_{in1} - G_3 V_{in1}^3. \qquad (18)$$

The first and second terms represent a fundamental signal and third-order distortion, respectively. The ratio of the fundamental to third-order distortion is given by

$$\frac{G_3}{G_1} = \frac{\beta}{8 I_{SS}} \propto \frac{1}{(V_{GS} - V_{th})^2}, \qquad (19)$$

where $V_{GS}$ is the gate-source bias voltage, and $V_{th}$ is the threshold voltage of the MOSFETs. To reduce the third-order distortion, the overdrive voltage, $V_{OV} \equiv V_{GS} - V_{th}$, need to be increased. On the other hand, the drain-source bias voltage, $V_{DS}$, must be larger than $V_{OV}$ to ensure that the MOSFETs operate in the saturation region. However, the drain bias voltage of the data-input MOSFETs is limited by the breakdown voltage. Therefore, to increase $V_{DS}$, decreasing the source bias voltage is required. The pseudo-differential switches shown in Fig. 4(c) cope with this requirement. $V_{DS}$ of the data-input MOSFETs can be increased by omitting the tail current source. As a result, the pseudo-differential switches enlarge $V_{OV}$, which reduces the third-order distortions.

Fig. 5 shows the schematic of the developed CMOS image-rejection AMUX with pseudo-differential switches. The data1 and data2 are switched by the clock1, and the data3 and data4 are switched by the clock2. The output currents of these switches are added based on Kirchhoff's current law at the output nodes of the AMUX. Let us discuss the effect of the third-order distortion on mid-band signal generation. Assuming the data input signals are normalized sinusoidal waves: $V_{\mathrm{in1}}(t) = \cos 2\pi f_{\mathrm{d}} t$ and $V_{\mathrm{in3}}(t) = \sin 2\pi f_{\mathrm{d}} t$, the output currents of the data1 and data3 are given by

$$\begin{aligned}&[I_{\mathrm{D1}}(t) - I_{\mathrm{D2}}(t)] \cdot s_{\mathrm{clk1}}(t)\\ &= A_1[+\cos 2\pi(f_{\mathrm{C}} + f_{\mathrm{d}})t + \cos 2\pi(f_{\mathrm{C}} - f_{\mathrm{d}})t] +\\ &\quad A_3[-\cos 2\pi(f_{\mathrm{C}} + 3f_{\mathrm{d}})t - \cos 2\pi(f_{\mathrm{C}} - 3f_{\mathrm{d}})t], \quad (20)\\ &\quad [I_{\mathrm{D7}}(t) - I_{\mathrm{D8}}(t)] \cdot s_{\mathrm{clk2}}(t)\\ &= A_1[-\cos 2\pi(f_{\mathrm{C}} + f_{\mathrm{d}})t + \cos 2\pi(f_{\mathrm{C}} - f_{\mathrm{d}})t] +\\ &\quad A_3[-\cos 2\pi(f_{\mathrm{C}} + 3f_{\mathrm{d}})t + \cos 2\pi(f_{\mathrm{C}} - 3f_{\mathrm{d}})t], \quad (21)\end{aligned}$$

where $A_1$ and $A_3$ are positive coefficients. Adding (20) and (21) rejects the terms of $(f_{\mathrm{C}} + f_{\mathrm{d}})$ and $(f_{\mathrm{C}} - 3f_{\mathrm{d}})$. A similar discussion holds for data2 and data4 by sign inversion. This result implies that the third-order distortion appears in the USB when the mid-band is generated, and it interferes with the high-band. Similarly, the third-order distortion appears in the LSB when the high-band is generated, and it interferes with the mid-band and low-band. Fig. 6 shows the simulated output spectrum when a sinusoidal wave is generated in the mid-band with different $V_{\mathrm{OV}}$. Fig. 6(a) and (b) are the cases without and with the tail current sources. The simulation was performed under the same gate and drain bias voltage of $V_{\mathrm{G,M1-4}}$=1.6 V and $V_{\mathrm{D,M1-4}}$=1.7 V were applied for data input MOSFETs. These bias voltages are limited by a breakdown voltage of the MOSFETs. When the clock input MOSFETs are 'ON' state, the source voltages of the data input MOSFETs are 0.8 V and 0.6 V in (a) and (b), respectively. Since the threshold voltage of the MOSFETs is about 0.46 V, the overdrive voltages of (a) and (b) are 0.34 V and 0.54 V. Increasing the overdrive voltage while using tail current sources does not work so well because it reduces the bias margin $V_{\mathrm{DS}} - V_{\mathrm{OV}}$. By omitting the tail current sources, larger overdrive voltage can be obtained and all the MOSFETs operate with a sufficient bias margin. The data input frequency $f_{\mathrm{M}}$ was 1 GHz, and the clock frequency $f_{\mathrm{C}}$ was 10 GHz. The target signal and third-order distortion appeared at 9 GHz (LSB) and 13 GHz (USB), which is consistent with the analytical result. In addition, increasing $V_{\mathrm{OV}}$ effectively reduces the third-order distortion.

Another signal degradation factor is noise. The noise performance of Gilbert cells in bandwidth multiplication techniques has not been considered conventionally (e.g., [17]). This is because the amplitudes of distortions and signals are sufficiently large compared to the noise, and the impact of noise on signal quality is small. On the other hand, the CMOS AMUX reported in this study has a smaller signal amplitude than bipolar ones, and it is becoming clear that noise affects the signal quality. This needs to be investigated in future research.

### *B. Broadband Termination*

The other challenge in the design of the CMOS AMUX is the bandwidth limitation. The bandwidth of the AMUX is determined at the output nodes because the output bandwidth is

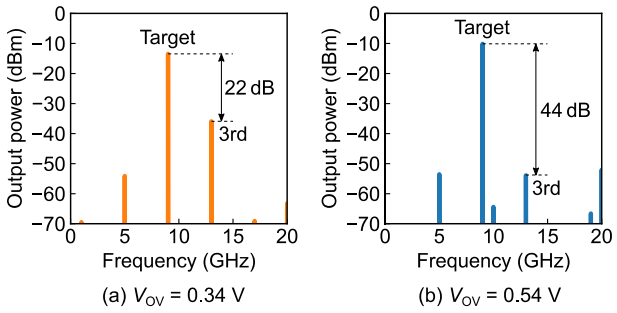



Fig. 6 Simulated output spectrum of the AMUX.

three times larger than the input bandwidth. However, the drain parasitic capacitances of the data input MOSFETs are summed at the output nodes, which degrades the bandwidth. To solve this problem, a broadband termination circuit with on-chip inductors and capacitors was devised and inserted into the output nodes. The termination circuit consists of $R_{\mathrm{T}}$, $L_1$, $L_2$, and $C_1$. The coupled inductors are used for $L_2$ to reduce the chip area. When the coupling coefficient of the inductors equals $k$, the inductance equals $(1 + k)L_2$ to the differential signals. Fig. 7 shows the equivalent of the termination circuit. $C_{\mathrm{D}}$ is the output parasitic capacitance of the switches. The inductors and capacitors form a two-stage LC ladder circuit. The resonance of the inductors and capacitors absorbs the parasitic capacitance like an artificial transmission line, which improves the matched bandwidth. The $L_1$ and $L_2$ also operate as shunt and series peaking inductors. Fig. 8 shows simulated output reflections for various termination circuits. The Smith chart has a marker at a frequency of 20 GHz. Adding the $L_1$, $L_2$, and $C_1$ brings the marker closer to the center of the Smith chart. When the device losses are ignored, adding the $L_2$ and $C_1$ moves output impedance along the constant resistance circle and constant conductance circle, respectively. Although adding the inductors and capacitors significantly rotate the phase of the reflection coefficients, this is not a problem because the magnitude of the reflection is sufficiently small. The −10 dB matched bandwidth for resistor-only termination is only 5.5 GHz. The devised termination circuit yields a matched bandwidth of 21.4 GHz that is 3.9 times greater than the resistor-only one. Fig. 9 shows the gain and phase responses from the data1 input to the output for various termination circuits. We found the flattest response for the devised termination circuit. It improves not only the reflection coefficients but also the gain and phase linearity at the expense of the slight series loss of $L_2$.

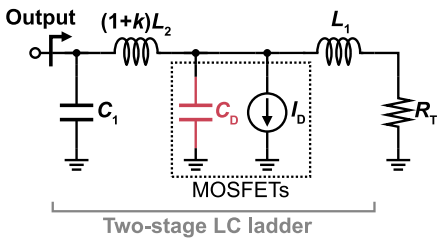



Fig. 7 Equivalent of the broadband termination circuit.

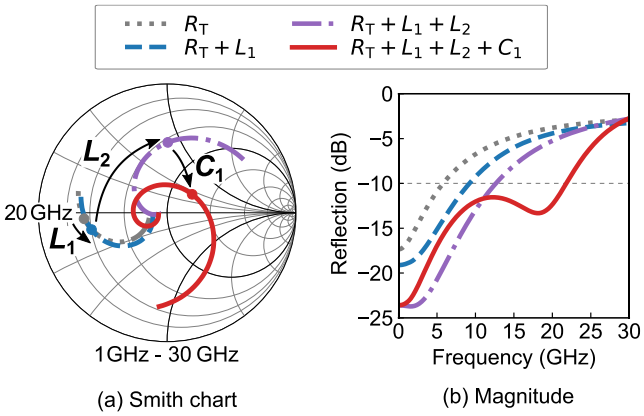



Fig. 8 Simulated output reflections of the AMUX.

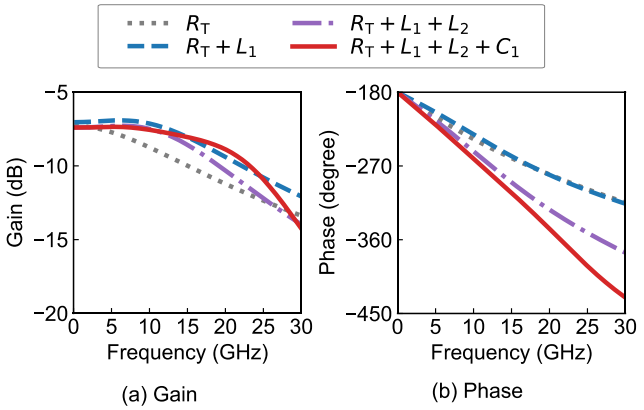



Fig. 9 Simulated gain and phase responses of the AMUX.

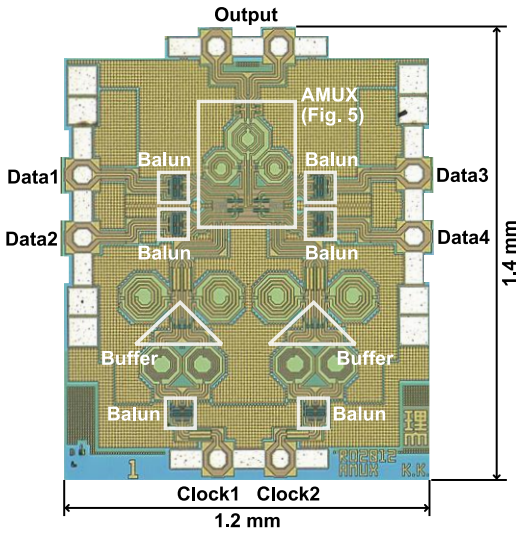



Fig. 10 Micrograph of the fabricated AMUX-IC.

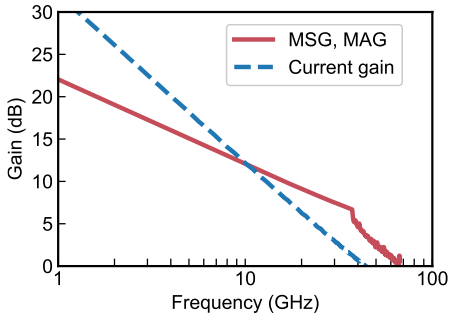



Fig. 11 Measured maximum stable gain (MSG), maximum available gain (MAG), and current gain of the MOSFET.

### *C. Implementation*

The AMUX was fabricated in Rohm's 1-poly 5-metal 180-nm CMOS process. Fig. 10 shows a micrograph of the fabricated AMUX-IC. The dimensions of all MOSFETs of the AMUX are $W/L = 64\ \mu m/0.18\ \mu m$ . Fig. 11 shows a measured maximum stable gain (MSG), maximum available gain (MAG), and current gain of the MOSFET up to 67 GHz. The test device was de-embedded from the RF pads by through-only method [28]. Both gate and drain bias voltage for measurement was 1.0 V, which was the gain maximum condition. The measured transition frequency $f_T$ and maximum oscillation frequency $f_{max}$ were approximately 45 GHz and 65 GHz, respectively. The broadband termination circuit is composed of poly resistors, spiral inductors with a top metal layer, and MIM (Metal-Insulator-Metal) capacitors. Active single-ended to differential conversion circuits (baluns) were inserted into all data and clock inputs to reduce the number of RF ports in experiments. The simulated bandwidth of the baluns is 8.9 GHz. The baluns have ultra-low gain and phase errors by using a feedback correction technique, and the detailed design is described in [29]. Buffers are also inserted into the clock inputs to amplify the weak output power of the baluns. The buffers are differential common-source amplifiers with series peaking at the input and shunt peaking at the output. The clock input paths have a simulated peak gain of 5 dB and a −3 dB bandwidth of 2–11 GHz. The baluns and buffers are not required when sub-DACs and an AMUX are monolithically integrated because the sub-DACs usually have differential output. The total chip area of the AMUX-IC is 1.7 $mm^2$, and the chip area of the AMUX excluding the baluns, buffers, and test pads is only 0.11 $mm^2$. The AMUX-IC operates with a CMOS compatible power supply of $V_{DD}$ = 2.2 V and a bias adjustment voltage of $V_T$ = 0.88 V. The total power consumption of the AMUX-IC is about 700 mW, and the power consumption excluding the baluns, buffers is 49 mW. These results suggest that monolithic integration can substantially reduce the chip areas and power consumption.

## IV. Measurement Results

The fabricated AMUX-IC was measured by on-chip probing to evaluate the performance. First, the frequency response of the AMUX was assessed by S-parameter measurements using a vector network analyzer. Next, the spurious performance was assessed by time-domain measurements using sinusoidal waves. Finally, broadband signal generation was demonstrated.

*A. Frequency-Domain Measurements*

The frequency responses of the AMUX excluding the baluns and buffers were measured with a four-port vector network analyzer Keysight PNA-X N5247B. Fig. 12(a) and (b) show the setup for the S-parameter measurements and its block diagram. The input for the data4 was connected to port 1 and port 3 of the network analyzer, and the output of the AMUX was connected to port 2 and port 4. The other data and clock inputs were terminated and biased via on-chip 50 Ω resistors. The bias voltage of the data input, $V_G$, was 1.6 V. The measurement frequency range was from 0.1 GHz to 30 GHz with a frequency step of 0.1 GHz. The measured 4-port S-parameters were converted into mixed-mode S-parameters after the measurements with scikit-rf version 0.21.0 [30], [31]. In addition, the input RF-pads and on-chip lead lines were eliminated by de-embedding using S-parameters obtained from the electromagnetic analysis. Fig. 13(a) shows the measured and simulated differential gain versus frequency. The measurement result demonstrated a peak gain of −8.3 dB and a −3 dB bandwidth of 23.4 GHz. Fig. 13(b) and (c) show the input and output reflection coefficients. The measured input and output −10 dB matched bandwidths were 16.3 GHz and 21.8 GHz, respectively. Despite the larger output parasitic capacitances, the wider output matched bandwidth was achieved compared with the input thanks to the broadband termination circuit. The in-out isolation is shown in Fig. 13(d). It was better than −20 dB across the measurement frequency range. Fig. 13(e) shows the group delay responses before and after de-embedding. The measured group delays were smoothed by moving averaging to reduce the measurement uncertainty. The measured group delay ripple was ±2.5 ps up to 15 GHz. The ripple near 1 GHz is due to the resonance of the parasitic inductance of the DC probes. In the time-domain measurements described below, this is not a problem because the much larger on-chip decoupling capacitor is installed

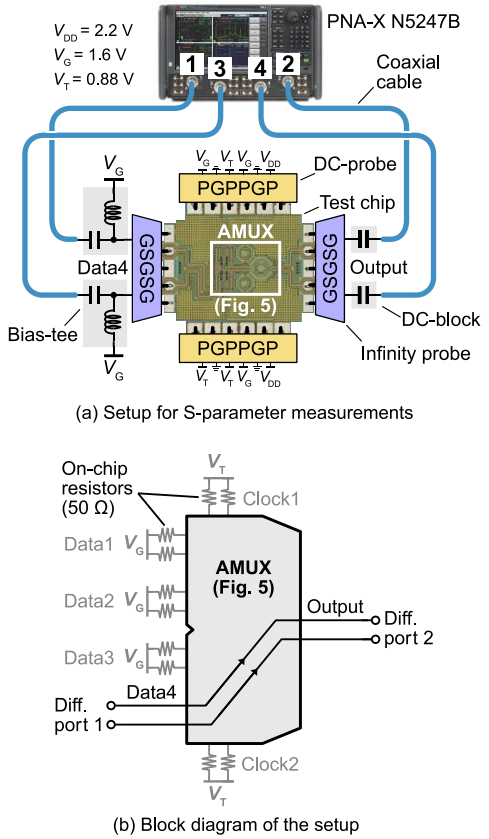



Fig. 12 Setup for S-parameter measurements.

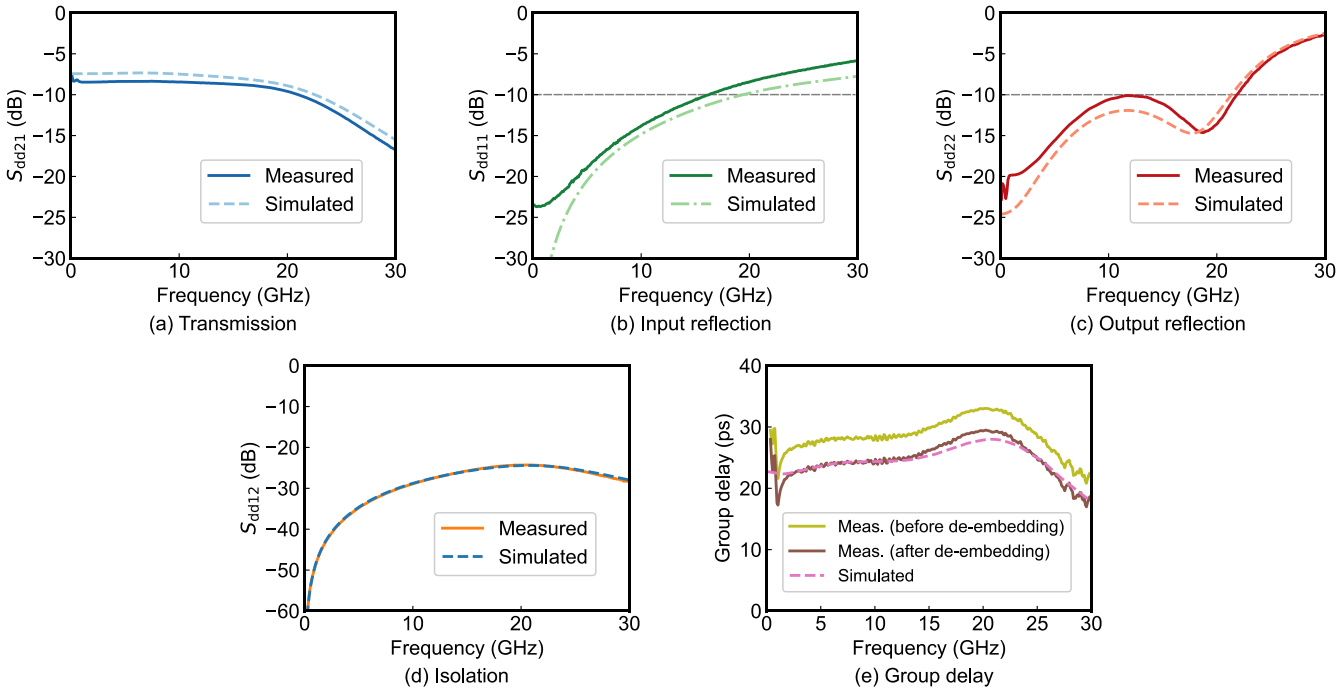
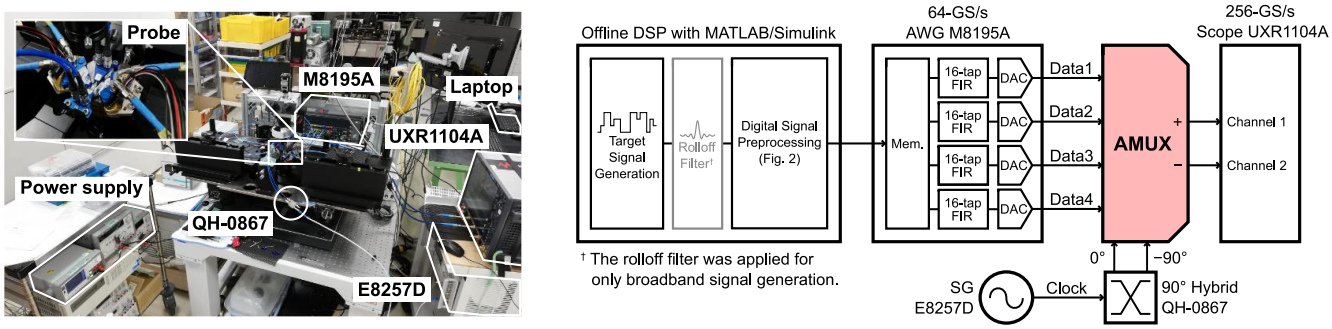



Fig. 13 Measured and simulated S-parameters.




(a) Measurement setup (b) Block diagram

Fig. 14 Setup for the time-domain measurements.

compared with the frequency-domain measurement. The measurement results agreed with simulation results, and we found that the AMUX was properly designed.

### *B. Time-Domain Measurements*

The spurious performance of the AMUX-IC including the baluns and buffers were assessed by time-domain measurements using sinusoidal waves. Fig. 14 shows a measurement setup and block diagram for the time-domain measurements. The input data signals were generated with a four-channel arbitrary waveform generator (AWG) Keysight M8195A in place of the sub-DACs. The sample rate of the AWG is 64 GS/s. The clock signals were generated with a signal generator (SG) Keysight E8257D and a 90° hybrid Marki QH-0867. The clock frequency was 10 GHz, and the clock amplitude was 400 mV at the probe tips. The differential output signals of the AMUX-IC were measured with a real-time oscilloscope Keysight UXR-1104A. The sample rate and analog bandwidth of the scope are 256 GS/s and 110 GHz. For the input/output wiring, phase-matched cables were used and contacted to the AMUX-IC using FormFactor Infinity probes. The input cables have delay mismatches of a few picoseconds, which causes significant data leakages. The delay mismatches were corrected using the built-in 16-tap finite impulse response (FIR) filters of the AWG to minimize the data leakages. Fig. 15 shows the measured and simulated third-order distortion ratios versus output power for the LSB and USB output. The input data frequency and clock frequency were $f_\mathrm{d}$ = 1 GHz and $f_\mathrm{C}$ = 10 GHz, and thus, the target frequency was 9 GHz and 11 GHz for the LSB and USB output, respectively. Although the measured distortions were about 5 dB worse than the simulation, a similar tendency was found. The worsening distortion ratio in the measurement is mainly due to the reduction in conversion gain caused by a gain reduction of the clock buffers. As discussed in Section III-A, the third-order distortions of the LSB and USB appear in the opposite sidebands. Since the distortion of the LSB is 2 to 3 dB larger than the USB, the high-band signal is more degraded than low- or mid-bands. The maximum output amplitude with a distortion ratio of less than −30 dB was −20 dBm for a 100-Ω differential load.

Fig. 16 shows sinusoidal output waveforms for various target frequencies. The data input amplitude was set to 300 mV at the output of the AWG so that the output amplitude was approximately −20 dBm. The amplitude for the thru was previously adjusted by a factor of $1/r = 1/8$. The scaling factor was determined using pilot signals so that the mid-band and low-band amplitudes were equal. The measured output amplitudes of the AMUX-IC were about 30 mV and 20 mV for $f_\mathrm{d}$ = 1 GHz and $f_\mathrm{d}$ = 4 GHz, respectively. The amplitude errors between these frequencies would be caused by the input bandwidth limitation due to the cables, probes, and baluns. In contrast, the amplitude errors between the sub-bands are very small, which enables broadband signal generation without equalization. Fig. 17 shows differential output spectrums. The thru output had a spurious-free dynamic range (SFDR) of over 40 dB. This is better than the LSB or USB because the input amplitude for thru is $r$ times smaller than the LSB or USB output. For the LSB and USB output, we found the data leakages at $f_\mathrm{d}$, clock leakages at $f_\mathrm{C}$, sideband leakages at $f_\mathrm{C} \pm f_\mathrm{d}$, and third-order distortions at $f_\mathrm{C} \pm 3f_\mathrm{d}$. The major determinant of the SFDR was the data leakages. Especially, higher $f_\mathrm{d}$ worsen the SFDR because the data leakages are caused by phase mismatch of the input signals. The third-order distortions were sufficiently small thanks to the pseudo-differential switches.

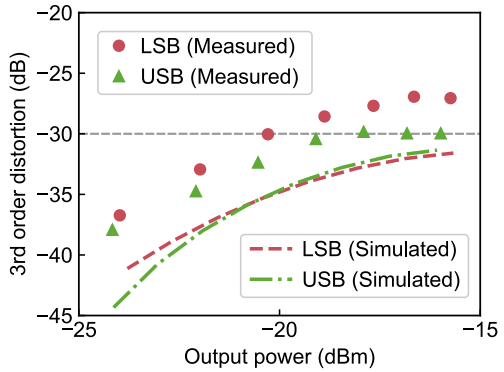
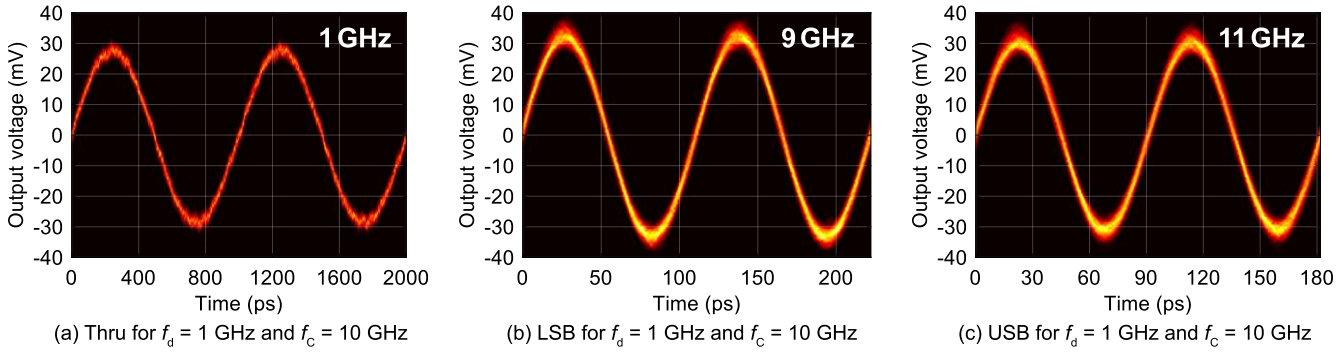


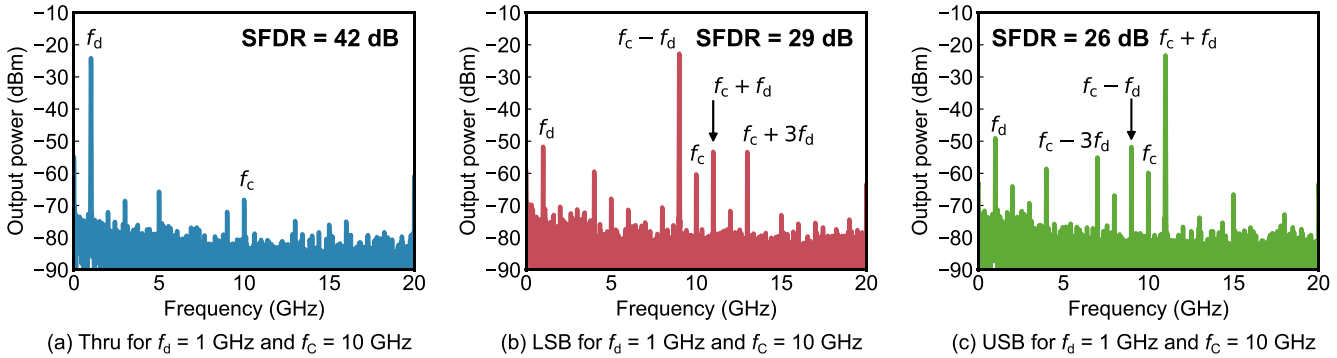

Fig. 15 Measured third-order distortion ratio versus output power.




(a) Thru for $f_d$ = 1 GHz and $f_C$ = 10 GHz (b) LSB for $f_d$ = 1 GHz and $f_C$ = 10 GHz (c) USB for $f_d$ = 1 GHz and $f_C$ = 10 GHz

(d) Thru for $f_d$ = 4 GHz and $f_C$ = 10 GHz (e) LSB for $f_d$ = 4 GHz and $f_C$ = 10 GHz (f) USB for $f_d$ = 4 GHz and $f_C$ = 10 GHz

Fig. 16 Measured differential output sinusoidal waveforms for various target frequencies.




(a) Thru for $f_d$ = 1 GHz and $f_C$ = 10 GHz (b) LSB for $f_d$ = 1 GHz and $f_C$ = 10 GHz (c) USB for $f_d$ = 1 GHz and $f_C$ = 10 GHz

(d) Thru for $f_d$ = 4 GHz and $f_C$ = 10 GHz (e) LSB for $f_d$ = 4 GHz and $f_C$ = 10 GHz (f) USB for $f_d$ = 4 GHz and $f_C$ = 10 GHz

Fig. 17 Measured differential output spectrums for various target frequencies.

*C. Broadband Signal Generation*

We demonstrated a broadband signal generation with the bandwidth tripler using the fabricated AMUX-IC. The measurement setup for the signal generation was the same as the spurious assessment as shown in Fig. 14. The modulation method of the target signal was PAM4, and the symbol rate was 15 Gbaud. The bandwidth of the target signal, $f_{\mathrm{m}}$, was limited using a raised cosine roll-off filter. The bandwidth of the roll-off filter is given by

$$f_{\mathrm{m}} = f_{\mathrm{N}}(1+\alpha), \quad [32] \qquad (22)$$

where $f_{\mathrm{N}}$ and $\alpha$ are the Nyquist frequency and roll-off factor. Here, we set $f_{\mathrm{N}}$ = 7.5 GHz and $\alpha$ = 1.0, and thus, the target bandwidth was 15 GHz as shown in Fig. 18(a). The bandwidth of the input data signals, $f_{\mathrm{B}} = f_{\mathrm{m}}/3$, was 5 GHz that corresponded with the bandwidth of the sub-DACs. The clock frequency, $f_{\mathrm{C}} = 2f_{\mathrm{m}}/3$, was 10 GHz. Fig. 18(b) and (c) shows the output spectrum of the AMUX-IC with and without the clock input. Without the clock input, the 5-GHz bandwidth spectrum was output without frequency conversion. With the clock input, the mid-band from 5 GHz to 10 GHz and the high-band from 10 GHz to 15 GHz were generated, and we found the broadband target spectrum with a bandwidth of 15 GHz. We found a peak at 16 GHz with an amplitude of about −70 dBm. The peak frequency corresponds to the integer fraction of the sampling frequency used for the measurement, and it could be due to sub-harmonic distortion in the sampling. Since the peak power is significantly lower than the target signal, it has small impact on the signal quality. Except for this peak, there was no image signal caused by input data signals out of the target bandwidth above 15 GHz despite not using analog filters at the output of the AMUX-IC. Fig. 19 shows an output eye diagram and vertical histogram. We generated a pseudo random bit sequence with the number of symbols of $2^{10}$ (= 1024). Then, the sequence was transmitted 11 times, thus the total number of transmitted bits is 11264 bits. A guard interval was inserted at the head of each sequence, and sequences did not affect each other. We found eye-opening for the 30 Gbps PAM4 signal. The differential peak-to-peak output amplitude was 60 mV. The measured root means squared error vector magnitude (RMS EVM) was −16.4 dB. The number of the detected transmission errors was 15 symbols out of 11264 symbols, and the bit error rate was $1.3\times10^{-3}$. The signal quality was degraded compared

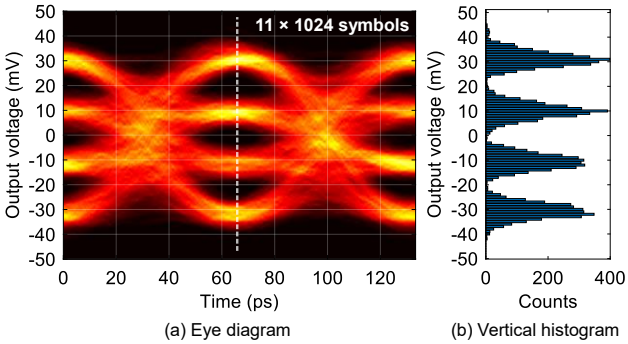



Fig. 19 Measured differential eye diagram and vertical histogram for 30-Gbps PAM4.

with the simulation results reported in [23]. We used a 50 Gbps PAM4 signal in the simulation with a roll-off factor of 0.2, but eye-opening could not be observed in the experiment under these conditions. Hence, the roll-off factor was increased to 1.0 and the data rate was reduced to 30 Gbps while keeping a clock frequency of 10 GHz. The larger roll-off factor provides a larger jitter margin, which reduces intersymbol interference. The first cause of the degradation of the signal quality is the lower SFDR reported in Fig. 17. As mentioned earlier, the deterioration in the SFDR is due to the gain reduction of the clock buffers, which can be improved by redesigning the clock buffers. The second cause is the frequency-dependent amplitude variation of the data input shown in Fig. 16. The eye diagram shows that the amplitude increases at the eye aperture, resulting in an overshoot. This is due to linear distortion at the data input, and thus, pre-equalization is effective to address this issue.

*D. Performance Comparison*

Table I lists the state-of-the-art AMUXs for performance comparison. The AMUXs presented in [10], [17] use InP DHBT technologies, which achieve superior symbol rates of 168 Gbaud and 100 Gbaud. These AMUXs also have a higher output swing thanks to an integrated output driver. These results suggest that InP technologies are well-suited for future broadband communication systems, except for their higher manufacturing costs. [11] and [12] use SiGe BiCMOS technologies that are feasible in aspects of the costs and

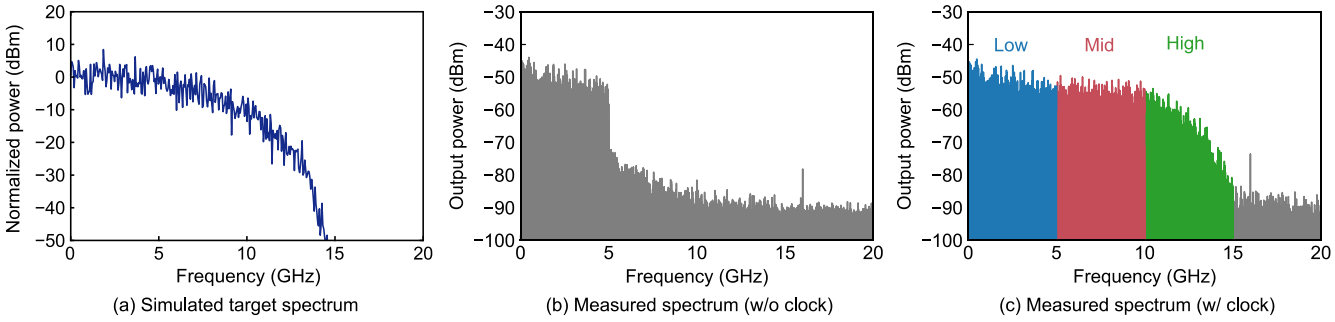



Fig. 18 Measured differential output spectrum for 30-Gbps PAM4.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART AMUXS

| Reference | This work | [17] 2020 J.SSC | [10] 2020 MIKON | [11] 2020 ECOC | [12] 2017 BCTM |
|---|---|---|---|---|---|
| **Technology** | 180-nm Si CMOS | 250-nm InP DHBT | 700-nm InP DHBT | 55-nm SiGe BiCMOS | 130-nm SiGe BiCMOS |
| **$f_T$ / $f_{max}$ (GHz)** | 45/65 | 460/480 | 340/410 | 325/375 | 300/500 |
| **Multiplication** | 3:1 | 2:1 | 2:1 | 2:1 | 2:1 |
| **Bandwidth (GHz)** | 23.4 (On-chip) | >110 (On-chip)<br>91 (Packaged) | N.R. | N.R. | >67 (On-chip) |
| **Out. swing ($V_{PPD}$)** | 0.06 | 1.5 | 0.9 | 0.7 | 0.75 |
| **Symbol rate (Gbaud)** | 15 (PAM4) | 168 (PAM4) | 100 (PAM4) | 100 (PAM8) | 56 (PAM4) |
| **Symbol rate / $f_{max}$** | 0.23 | 0.35 | 0.24 | 0.27 | 0.11 |
| **Supply voltage (V)** | 2.2 | −4.5 | N.R. | −5.7 | −4.5 |
| **Power (mW)** | 49†/130‡/700‡‡ | 990 | N.R. | 2166 | 1060 |
| **Efficiency (pJ/bit)** | 1.6†/4.3‡/23‡‡ | 2.9 | N.R. | 5.4 | 9.5 |
| **Chip-area ($mm^2$)** | 0.11†/1.7‡‡ | 4 | 1.8 | N.R. | 1.6 |

†AMUX, ‡AMUX and clock buffers, ‡‡Whole chip.

TABLE II
COMPARISON WITH THE CUTTING-EDGE CMOS DACS

| Reference | This work | [3] 2021 ISSCC | [4] 2019 BCICTS | [5] 2017 ISSCC | [6] 2015 ISSCC | [7] 2015 T-MTT |
|---|---|---|---|---|---|---|
| **Technology** | 180-nm standard | 7-nm FinFET | 7-nm FinFET | 20-nm standard | 28-nm standard | 28-nm low-power |
| **Architecture** | AMUX | CML | CML | CML | CML | CML |
| **Sample rate (GS/s)** | N/A* | 40–97 | 60 | 64 | 18 | 100 |
| **Bandwidth (GHz)** | 23.4 | 40 | N.R. | 20 | >9 | 13 |
| **Data rate (Gbps)** | 30** (PAM4) | 132 (PAM4) | N.R. | 64 (NRZ) | 36** (PAM4) | 120 (PAM8) |
| **SFDR (dB)** | 40 (4 GHz)<br>22 (6 GHz)<br>20 (14 GHz) | 51 (0.1 GHz)<br>41 (30 GHz) | 30 (20 GHz) | 50 (1 GHz)<br>40 (14.7 GHz) | 52 (0.7 GHz)<br>43 (8 GHz) | 37 (0 Hz)<br>27 (<20 GHz) |
| **Supply voltage (V)** | 2.2 | 1.8 | 1.9 | N.R. | 1.5 | 2 |

*Depending on the sub-DACs, **No equalization has been reported.

performance. The AMUX described in [11] has the highest linearity and resolution at the expense of the power consumption, achieving 100-Gbuad PAM8 signal generation that is the highest data rate.

The developed AMUX in this work achieves three-to-one multiplication. Besides, this is the first demonstration of the CMOS AMUX developed for optical transmitters to the best of the authors' knowledge. The power consumption excluding the baluns is lower than the previous work, achieving superior power efficiency. The symbol rate normalized by $f_{max}$ is in line with previous ones, which implies that the developed techniques could be applied to the advanced CMOS technology to obtain the compatible bandwidth with InP or SiGe technologies.

Table II lists the cutting-edge CMOS DACs with advanced CMOS technologies. All previous studies listed in the table use the CML architecture. These DACs provide resolutions up to 8-bit, and they are available for the sub-DACs in the AMUX architecture. The developed AMUX has a comparable bandwidth to the CML-based DACs with advanced CMOS technologies despite using a 180-nm process. Therefore, the AMUX architecture achieves higher bandwidth compared with the conventional DAC architectures. The next tasks are to improve the SFDR and integration with sub-DACs and photonic devices.

## V. CONCLUSION

This paper presented a bandwidth tripler with a CMOS

image-rejection AMUX for optical transmitters. The tripler extends the bandwidth of the parallelized sub-DACs by three times using digital signal preprocessing and analog multiplication. The tripler does not generate any image signal out of the bandwidth thanks to the image rejection. Besides, the tripler does not require analog filters, which improves the signal quality and manufacturing costs. The AMUX was fabricated in a 180-nm CMOS process. The CMOS-based AMUX reduces power consumption, footprints, and manufacturing costs by integrating with digital circuits, sub-DACs, and silicon photonics devices. The pseudo-differential switches were used to reduce the distortions, the output matched bandwidth was improved by 3.9 times with a broadband termination circuit. The measured bandwidth of the AMUX was 23.4 GHz that is comparable to the CML-based DACs fabricated in advanced CMOS technologies. Furthermore, measurement results demonstrated a 30 Gbps PAM4 broadband signal generation. Therefore, the bandwidth tripler and the developed AMUX improve the bandwidth, manufacturing costs, and power efficiency of optical transmitters.

## ACKNOWLEDGMENT

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