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A 0.0058-mm^2 Inductor-Less CMOS Active Balun With Gain and Phase Errors Within −0.1±0.2 dB and −0.18±1.17° From DC to 8 GHz

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***Abstract*— This paper presents a low-imbalance and inductor-less active balun. The large immittance of the parasitics increases gain and phase errors in single-ended-to-differential conversion at high frequencies. Positive feedback is effective in reducing these errors. However, there is a trade-off between the stability of the feedback and the imbalance correction. This paper analyzes this trade-off, and the common-mode rejection ratio (CMRR) was improved by adding a capacitor. Besides, we established the feedback loops for the imbalance correction are also available for bandwidth extension, that is the additional capacitor improves not only the CMRR but also the high-frequency gain. This peaking technique removes inductors that consume large chip areas. The balun was fabricated in a 0.18-µm CMOS process and achieved a small core area of 0.0058 mm^2. In addition, a self-bias scheme using a current mirror was devised. It ensures a good bias current balance and reduces errors. The manufacturing variation of the fabricated baluns was statistically evaluated. To obtain the 99.7% limit of the CMRR, we extended the theory of the random CMRR to the complex plane. The measurement results demonstrated small errors within −0.1±0.2 dB and −0.18±1.17° including a variation of ±3σ from DC to 8.0 GHz.**

***Index Terms*—Balun, active balun, imbalance correction, active feedback, gain error, phase error, process variation, CMRR, random CMRR, CMOS, integrated circuit.**

I. Introduction

CLOUD computing using big data has led to a rapid increase in communication traffic. High-speed and high-capacity optical fiber backbone networks are essential for processing considerable amounts of information. Several frequency interleaving techniques using analog multiplication have been reported to increase the bandwidth of optical fiber communications [1]–[4]. The multiplication is performed by an integrated circuit based on Gilbert cells. Gilbert cells typically have a differential configuration and require multiple high-frequency input/output ports. For example, a multiplexer previously reported by our group requires six input ports and one output port in a differential configuration [3]. This aspect causes difficulties in layout design, packaging, and measurement evaluation. Some studies integrated baluns that convert single-ended signals to differential signals to reduce the number of ports [3], [4]. The baluns for the multiplexers require wider operation bandwidth with DC coupling. Active baluns are suitable for multiplexers because they can have small excess insertion loss from DC to high frequencies. However, the circuit topology asymmetry and large parasitic immittances cause errors in the gain and phase of the differential output. These errors degrade the sideband-suppression ratio in multiplexing and considerably affect signal quality. The error can be classified into systematic and random errors. The systematic error has statistical correlations among the multiple fabricated chips, while the random error does not. The primary cause of the systematic error is the asymmetry in circuit topology or layout, and that of the random error is process variation. Fig. 1 shows various error-correction techniques reported in the previous studies. The active balun is composed of inverting and non-inverting amplifiers, typically in a common source and common gate (CS-CG) structure [5]–[13] or a common source and common drain (CS-CD) structure [14]–[16]. The CS-CG structure is widely used in wireless communications as a noise-canceling amplifier. The common source circuits have a longer delay time than common gate or drain circuits due to the Miller effect. Fig. 1(a) shows a circuit that uses a cascode transistor to compensate for this delay mismatch [13]. Similarly, Fig. 1(b) shows a circuit that uses a common gate buffer for delay matching and DC level shifting [17]–[22]. This topology is also known as a source-coupled pair. Common-mode rejection ratio (CMRR) can be improved by inserting inductive reactance into the source node of M6

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[21]. Another method for delay matching is inserting a transmission line as a delay element. Stärke *et al*. [22] have inserted transmission lines and a common gate buffer. Although these correction techniques are simple and easy to design, they can cause an imbalance due to modeling errors or process variation. Fig. 1(c) shows the phase correction technique that cancels the imbalance of Balun-A with cross-coupled CS-CG buffers [23]–[26]. A similar technique using a CS-CD structure has been reported in [27]. Assuming that the phase errors due to Balun-A and the mismatch between CS-CG buffers are $\Delta\theta_A$ and $\Delta\theta_B$, respectively, the output currents from M7 to M10 are given as follows [23].

$$\begin{cases} I_7 = \sin\omega t, \\ I_8 = \sin(\omega t + \Delta\theta_A + \Delta\theta_B), \\ I_9 = -\sin(\omega t + \Delta\theta_B), \\ I_{10} = -\sin(\omega t + \Delta\theta_A). \end{cases} \quad (1)$$

From (1), the currents injected into the load are given by

$$I_7 + I_8 = 2\cos\left(\frac{\Delta\theta_A + \Delta\theta_B}{2}\right)\sin\left(\omega t + \frac{\Delta\theta_A + \Delta\theta_B}{2}\right), \quad (2)$$

$$I_9 + I_{10} = -2\cos\left(\frac{\Delta\theta_A - \Delta\theta_B}{2}\right)\sin\left(\omega t + \frac{\Delta\theta_A + \Delta\theta_B}{2}\right). \quad (3)$$

The phase error can be corrected when there is no gain error in the CS-CG buffers and Balun-A. However, this ideal operation cannot be realized in the practical design because they have some gain errors. The gain and phase errors in the 60-GHz band are limited to 1.7 dB and 6.8°, respectively [23]. Fig. 1(d) shows the magnitude and phase concurrent correction technique (MPCCT) that improves on this drawback [28]. Chou *et al.* demonstrated gain and phase errors of 0.36 dB and 2.2° in the 60-GHz band with MPCCT. In the MPCCT, positive and negative feedback paths are added to the phase correction technique. The positive feedback loop composed of M11 and M14 corrects the gain and phase errors concurrently. A similar technique to remove common-mode voltage by positive feedback includes Nauta's operational transconductance amplifier (OTA) [29]. Infinite CMRR is obtained when the loop gain of the positive feedback equals one; however, it causes a stability problem. The loop gain should be less than one for stability, which reduces the effectiveness of the correction. A quantitative evaluation of these concessions is necessary to achieve a large CMRR and stable operation. In this study, we analyzed the relationship between the gain margin of the positive feedback and the CMRR. The analysis provided the theoretical limits of the CMRR obtained by the positive feedback. Furthermore, based on the analysis, we adjusted the loop gain by adding a capacitor, thus improving the CMRR. In addition, we established that the positive and negative feedback in the MPCCT are also available for active peaking. The additional capacitor improves not only the CMRR but also the high-frequency gain, thereby enhancing the gain bandwidth product and reducing the chip area.

This paper is an extended version of [30]. We have added a plausible description of the MPCCT by node impedance analysis. Besides, we derived *S*-parameters when a current mirror is used for the input balun. The measured gain and phase errors were statistically evaluated, including the process variation. This paper is organized as follows: Section II describes the analysis; Sections III and IV provide the simulation and measurement results; Section V concludes the paper.

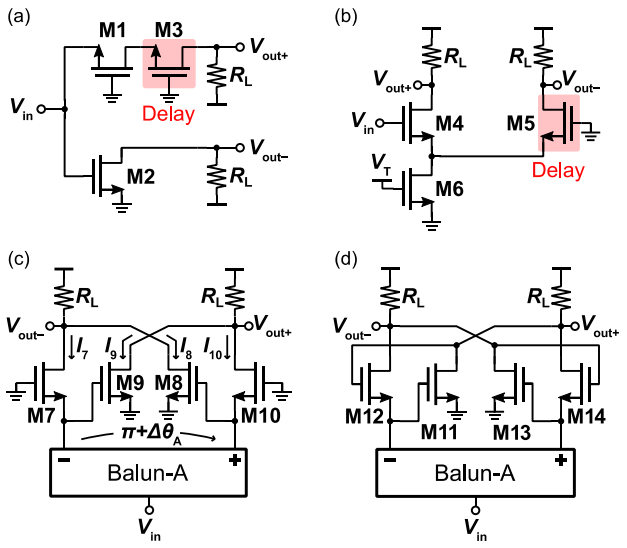


Fig. 1. Various error correction techniques reported in the previous studies. (a) Common source and common gate structure with a cascode transistor. (b) Source coupled pair. (c) Phase correction technique. (d) Magnitude and phase concurrent correction technique.

II. Analysis

A. Magnitude and Phase Concurrent Correction

Fig. 2 shows a simplified schematic and block diagram of the feedback loops in the MPCCT. The definitions of i_{o1} and i_{o2} were modified from [28] and [30] so that the block diagrams and schematics correspond exactly. For simplicity, the analysis ignores the feedforward path of C_N. The correction circuit is composed of one positive feedback loop and two negative feedback loops. Among these feedback loops, the positive feedback loop contributes to error correction. $A = Z_L$ represents an open-loop transimpedance gain. $\beta_p^{\pm}$ and $\beta_n^{\pm}$ represent feedback factors of the positive and negative feedback at the plus and minus sides of Balun-A. The output impedance at the plus and minus sides of Balun-A are generally not equal, the feedback factors are also different values for the plus and minus sides. The output voltage v_{o1} and v_{o2} are given by [28]

$$v_{o1} = \frac{1}{\delta}\left[\left(\frac{1}{A} + \beta_n^-\right) i_{o1} - \beta_p^- i_{o2}\right], \quad (4)$$

$$v_{o2} = -\frac{1}{\delta}\left[\beta_p^+ i_{o1} - \left(\frac{1}{A} + \beta_n^+\right) i_{o2}\right], \quad (5)$$

where δ is defined as

$$\delta = \left(\frac{1}{A} + \beta_n^-\right)\left(\frac{1}{A} + \beta_n^+\right) - \beta_p^- \beta_p^+. \quad (6)$$

The conditions for the coefficients on the right-hand sides of (4) and (5) to be equal are

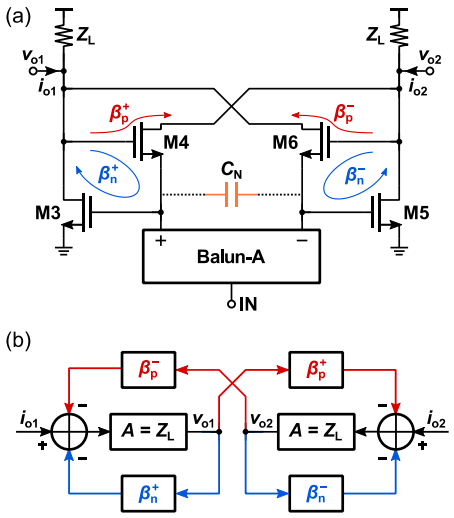


Fig. 2. Positive and negative feedback loops in the MPCCT. (a) Simplified schematic. (b) Block diagram.

$$\frac{1}{A} + \beta_{\mathrm{n}}^{\pm} = \beta_{\mathrm{p}}^{\mp}, \tag{7}$$

where double sign corresponds. When (7) holds, v_{o1} and v_{o2} differ only in sign, which means that the output becomes a perfect differential voltage. However, it causes oscillation when the loop gain of the positive feedback reaches one. The gain margin for stable operation reduces the effectiveness of the correction. This study clarifies the relationships between the gain margin and CMRR. The output common-mode voltage v_{com} and differential voltage v_{dif} are defined as

$$v_{\mathrm{com}} = \frac{v_{\mathrm{o1}} + v_{\mathrm{o2}}}{2}, \tag{8}$$

$$v_{\mathrm{dif}} = \frac{v_{\mathrm{o1}} - v_{\mathrm{o2}}}{2}. \tag{9}$$

Substituting (4) and (5) into (8) and (9), we obtain

$$v_{\mathrm{com}} = \frac{1}{\delta} \cdot \frac{\left(\frac{1}{A} + \beta_{\mathrm{n}}^{-} - \beta_{\mathrm{p}}^{+}\right) i_{\mathrm{o1}} + \left(\frac{1}{A} + \beta_{\mathrm{n}}^{+} - \beta_{\mathrm{p}}^{-}\right) i_{\mathrm{o2}}}{2}, \tag{10}$$

$$v_{\mathrm{dif}} = \frac{1}{\delta} \cdot \frac{\left(\frac{1}{A} + \beta_{\mathrm{n}}^{-} + \beta_{\mathrm{p}}^{+}\right) i_{\mathrm{o1}} - \left(\frac{1}{A} + \beta_{\mathrm{n}}^{+} + \beta_{\mathrm{p}}^{-}\right) i_{\mathrm{o2}}}{2}. \tag{11}$$

The common-mode voltage becomes smaller than the differential voltage even if the feedback factors at the plus and minus sides were different. Assuming $\beta_{\mathrm{n}} = \beta_{\mathrm{n}}^{+} \approx \beta_{\mathrm{n}}^{-}$ and $\beta_{\mathrm{p}} = \beta_{\mathrm{p}}^{+} \approx \beta_{\mathrm{p}}^{-}$, the output node impedance for common- and differential-modes is given by

$$Z_{\mathrm{com}} = \frac{1}{\frac{1}{A} + \beta_{\mathrm{n}} + \beta_{\mathrm{p}}} \tag{12}$$

$$Z_{\mathrm{dif}} = \frac{1}{\frac{1}{A} + \beta_{\mathrm{n}} - \beta_{\mathrm{p}}} \tag{13}$$

Therefore, the node impedance for differential-mode is larger than for common-mode, which provides common-mode rejection similar to Nauta's OTA [29]. The CMRR obtained by the positive feedback of the MPCCT is given by

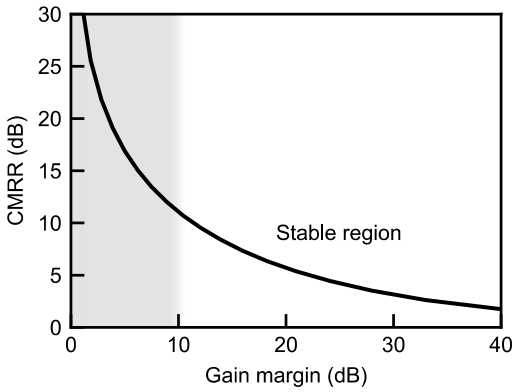


Fig. 3. Trade-off between the CMRR and gain margin.

$$CMRR_{\mathrm{MPCCT}} = \frac{\frac{1}{A} + \beta_{\mathrm{n}} + \beta_{\mathrm{p}}}{\frac{1}{A} + \beta_{\mathrm{n}} - \beta_{\mathrm{p}}} = \frac{1 + \sqrt{A_{\mathrm{loop}}}}{1 - \sqrt{A_{\mathrm{loop}}}}, \tag{14}$$

where A_{loop} represents the loop gain of the positive feedback defined as

$$A_{\mathrm{loop}} = \left(\frac{A\beta_{\mathrm{p}}}{1 + A\beta_{\mathrm{n}}}\right)^2. \tag{15}$$

Fig. 3 shows the relationship between the gain margin and CMRR obtained from (14). The gain margin was calculated by a reciprocal of A_{loop}. As discussed earlier, increasing A_{loop} increases the CMRR. Empirically, the recommended gain margin is over 10 dB [32], which limits the CMRR up to 10 dB. From (15), to increase A_{loop}, the negative feedback should be weakened, and the positive feedback should be strengthened. In this study, we inserted a capacitor C_{N} into the output of Balun-A as shown in Fig. 2(a). C_{N} reduces the output impedance of Balun-A, which weaken the negative feedback and strengthen the positive feedback at high frequencies. The CMRR can be improved by increasing the loop gain. We confirmed the effect of C_{N} by simulation described in Section III.

B. Practical Analysis of the MPCCT

In this subsection, we derive transfer functions for the positive and negative feedback factors and formulate the impact of C_{N} on CMRR and gain margin. Assuming that the output conductance of Balun-A is equal to G_{A} for plus and minus outputs, β_{n} and β_{p} are given by

$$\beta_{\mathrm{n}} = \frac{g_{\mathrm{m5}} g_{\mathrm{m6}}}{(g_{\mathrm{m6}} + G_{\mathrm{A}}) + 2C_{\mathrm{N}}s}, \tag{16}$$

$$\beta_{\mathrm{p}} = \frac{g_{\mathrm{m6}} G_{\mathrm{A}} + 2g_{\mathrm{m6}} C_{\mathrm{N}} s}{(g_{\mathrm{m6}} + G_{\mathrm{A}}) + 2C_{\mathrm{N}}s}. \tag{17}$$

where g_{m5} and g_{m6} represent the transconductance of M5 and M6. Although the parasitic capacitances of the transistors also affect the transfer function, we considered only the added capacitor C_{N} for simplicity. β_{n} and β_{p} are a first-order lag element

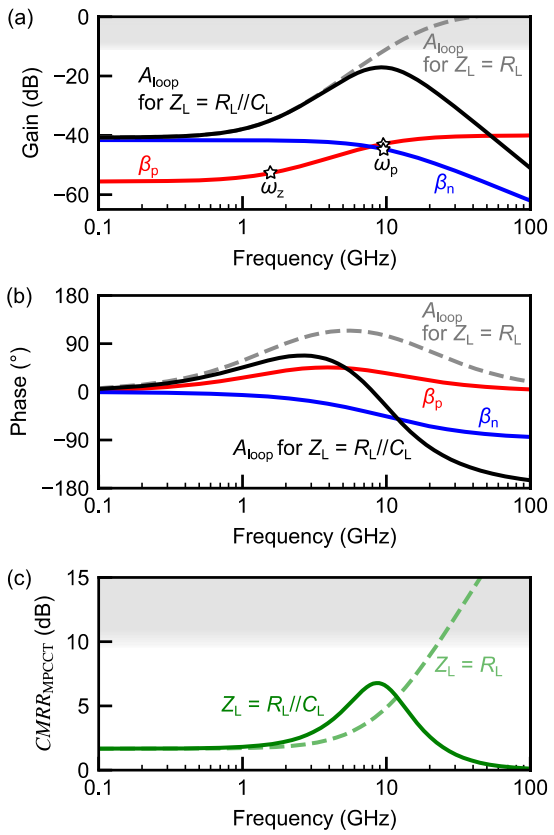


Fig. 4. Calculated Bode plots for $g_{m5} = g_{m6} = 10$ mS, $G_A = 2$ mS, $C_N = 100$ fF, $C_L = 300$ fF, $R_L = 110$ Ω. (a) Gain and (b) phase of β_n, β_p, and A_{loop}. (c) Magnitude of $CMRR_{MPCCT}$.

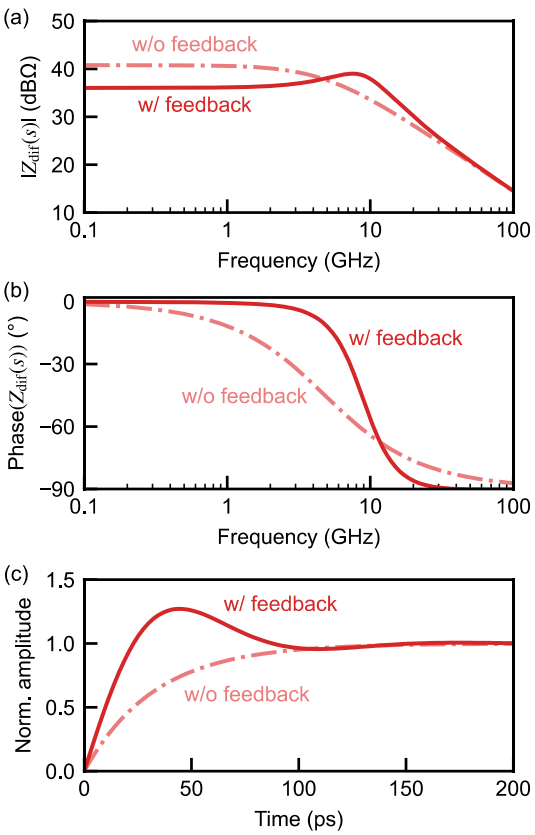


Fig. 5. Calculated output node impedance for differential mode and its step response with and without feedback for $g_{m5} = g_{m6} = 10$ mS, $G_A = 2$ mS, $C_N = 100$ fF, $C_L = 300$ fF, $R_L = 110$ Ω. (a) Magnitude of $Z_{dif}(s)$. (b) Phase of $Z_{dif}(s)$. (c) Step response.

and phase compensation element with a pole at ω_p and a zero at ω_z, respectively. ω_p and ω_z are given by

$$\omega_p = \frac{g_{m6} + G_A}{2C_N}, \tag{18}$$

$$\omega_z = \frac{G_A}{2C_N}. \tag{19}$$

Substituting (16) and (17) into (14) and (15), we obtain

$$CMRR_{MPCCT} = \frac{\left[g_{m6}(g_{m5} + G_A) + \frac{g_{m6} + G_A}{Z_L}\right] + 2C_N\left(\frac{1}{Z_L} + g_{m6}\right)s}{\left[g_{m6}(g_{m5} - G_A) + \frac{g_{m6} + G_A}{Z_L}\right] + 2C_N\left(\frac{1}{Z_L} - g_{m6}\right)s} \tag{20}$$

$$\sqrt{A_{loop}} = \frac{g_{m6}G_A Z_L + 2g_{m6}C_N Z_L s}{(g_{m6} + G_A + g_{m5}g_{m6}Z_L) + 2C_N s} \tag{21}$$

Fig. 4 shows calculated Bode plots of the feedback factors, loop gain, and CMRR. The element values used in the calculation were rough approximations of the design described below. Since the parasitic capacitance of the MOSFETs works in the same way as C_N, the value of C_N in the calculation was larger than the capacitance actually added. $|\beta_n|$ is decreased and $|\beta_p|$ is increased at high frequencies, and therefore, the positive feedback becomes dominant, and large $|A_{loop}|$ is achieved. The dashed lines in Fig. 4 represent A_{loop} and $CMRR_{MPCCT}$ when $Z_L = R_L$. Although $CMRR_{MPCCT}$ diverges to large values at high frequencies, the gain margin falls below 10 dB. The solid black and green lines show A_{loop} and $CMRR_{MPCCT}$ when $Z_L = R_L // C_L$. C_L represents load capacitance including the parasitics of the balun and next stage. The poles generated by the C_L limit $|A_{loop}|$, ensuring a sufficient gain margin. This also limits the $CMRR_{MPCCT}$ to less than 10 dB, which causes a peak response at high frequencies.

C. Active Peaking

Another challenge in designing broadband active baluns is to reduce the chip area. Inductive elements are usually used for bandwidth extension, for example, shunt peaking [32], series peaking [33]–[35], and T-coil peaking [36]–[37]. The more inductors used; the wider bandwidth is achieved [38]–[40]. They, however, consume large chip areas. Active peaking is known as a bandwidth extension technique that does not require inductive elements [41]. Qualitatively, an active circuit produces negative feedback at low frequencies and positive feedback at high frequencies to extend the bandwidth by decreasing the low-frequency gain and increasing the high-frequency gain. Since inductors are not used, a small area is achieved. The combination of active feedback and inductive peaking also provides an excellent small area, such as bridged shunt grounded active inductor (GAI) peaking [42]. In this study, we established that the positive and negative feedback in the MPCCT is also available for active peaking. The proposed peaking method embedded in

the MPCCT does not require any additional inductors or transistors, and thus achieves a small area and low power consumption. First, we assume the dominant pole is placed at the output nodes of the MPCCT, and all bandwidth limitation due to the other nodes is ignored. The frequency response without active peaking is determined by the impedance of the output node $Z_{\mathrm{L}}(s) = R_{\mathrm{L}} \,//\, C_{\mathrm{L}}$. This is a simple first-order lag element, and the 3-dB bandwidth is given by $1/2\pi R_{\mathrm{L}}C_{\mathrm{L}}$. Substituting (16), (17), and $A = R_{\mathrm{L}} \,//\, C_{\mathrm{L}}$ into (13), we obtain (22): a transfer function of the output node impedance for differential signals indicated at the bottom of this page. $Z_{\mathrm{dif}}(s)$ has two poles and one zero, which is the same as shunt peaking. Fig. 5 shows the calculated frequency response of $Z_{\mathrm{dif}}(s)$ with and without active peaking embedded in the MPCCT. At low frequencies, the impedance is reduced due to the negative feedback, and at high frequencies, the impedance is increased due to negative impedance conversion for C_{N} by the positive feedback. As a result, the frequency response is flattened as shown in Fig. 5(a) and (b), and the transient time is improved as shown in Fig. 5(c). The transfer function (22) shows that a larger g_{m} reduces the low-frequency gain, and a larger C_{N} enhances peaking. Therefore, the added capacitor C_{N} improves both CMRR and bandwidth. However, too large C_{N} causes excessive overshoot. The designer must strike a balance between the CMRR, frequency response, and stability.

D. Self-Biasing With a Current Mirror

Fig. 6 shows a full schematic of the developed balun. Conventionally, Balun-A consists of a fixed-bias two-stage common source amplifier [23], [24] or differential pair [25], [26]. The fixed-bias amplifier requires a DC cut capacitor that degrades low-frequency performance. For the differential pair, a low-voltage operation is difficult because the transistors are stacked in three stages. In addition, an additional bias voltage must be provided in both cases. To deal with these challenges, we used a current mirror for Balun-A. The bias currents of M1 to M6 are self-biased to equal values. For example, assuming that the bias current of M5 is larger than that of M3, the gate voltage of M6 should be smaller than that of M4. However, the gate-source voltages of M4 and M6 are equal because the current mirror provides the same bias current to M4 and M6. Consequently, the gate voltage of M5 is smaller than that of M3, which contradicts the previous assumption. The same is true when the bias current of M5 is assumed to be smaller than that of M3. Therefore, this biasing scheme achieves a better balance of the bias currents without using external bias voltage and DC cut capacitors. This ensures transistor characteristic matching and reduces the gain and phase errors. Although slightly larger currents flow in M3 and M5 due to the channel length modulation, no imbalance is caused because symmetricity is still maintained. The drawback of using a current mirror is that it causes an imbalance in the output impedance of Balun-A. To investigate this effect, a small-signal analysis was performed; since the

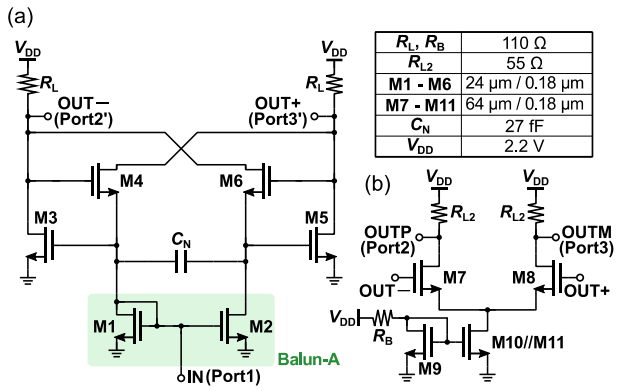


Fig. 6. Full schematic of the balun. (a) Balun core. (b) Output buffer.

negative feedback loop of the MPCCT is parallel-parallel feedback, the *S*-parameters were derived via the *Z*-parameters, which are more easily analyzed. The three port *Z*-parameters, excluding the output buffer at low frequencies, are given by

$$Z_{11} = \frac{1}{2g_{\mathrm{m}}} \cdot \frac{1}{1 + g_{\mathrm{m}}R_{\mathrm{L}}}, \tag{23}$$

$$Z_{2'2'} = Z_{3'3'} = -Z_{2'1} = Z_{3'1} = \frac{R_{\mathrm{L}}}{1 + g_{\mathrm{m}}R_{\mathrm{L}}}, \tag{24}$$

$$Z_{12'} = \frac{1}{2} \cdot \frac{R_{\mathrm{L}}}{1 + g_{\mathrm{m}}R_{\mathrm{L}}}, \tag{25}$$

$$Z_{13'} = Z_{2'3'} = Z_{3'2'} = 0, \tag{26}$$

where the transconductance of M1 to M6 is equal to g_{m}, and the output resistance of the transistor was neglected for simplicity. The port numbers with apostrophes are indicated in Fig. 6(a). Note that the positive feedback can be neglected at low frequencies because M2 has a high output resistance. Assuming 1-Ω reference impedance for all ports, the *Z*-parameters are converted to the *S*-parameters as follows.

$$S_{11} = \frac{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 - 2R_{\mathrm{C}} - 2) + R_{\mathrm{C}}^2 + R_{\mathrm{C}}}{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 + 2R_{\mathrm{C}} + 2) + R_{\mathrm{C}}^2 + R_{\mathrm{C}}}, \tag{27}$$

$$S_{2'2'} = \frac{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 + 2R_{\mathrm{C}} - 2) + R_{\mathrm{C}}^2 - R_{\mathrm{C}}}{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 + 2R_{\mathrm{C}} + 2) + R_{\mathrm{C}}^2 + R_{\mathrm{C}}}, \tag{28}$$

$$S_{3'3'} = \frac{R_{\mathrm{C}} - 1}{R_{\mathrm{C}} + 1}, \tag{29}$$

$$-S_{2'1} = S_{3'1} = \frac{4g_{\mathrm{m}}R_{\mathrm{L}}R_{\mathrm{C}}}{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 + 2R_{\mathrm{C}} + 2) + R_{\mathrm{C}}^2 + R_{\mathrm{C}}}, \tag{30}$$

$$S_{12'} = \frac{2g_{\mathrm{m}}R_{\mathrm{L}}R_{\mathrm{C}}}{g_{\mathrm{m}}R_{\mathrm{L}}(R_{\mathrm{C}}^2 + 2R_{\mathrm{C}} + 2) + R_{\mathrm{C}}^2 + R_{\mathrm{C}}}, \tag{31}$$

$$Z_{\mathrm{dif}}(s) = \frac{(g_{\mathrm{m6}}R_{\mathrm{L}} + G_{\mathrm{A}}R_{\mathrm{L}}) + 2R_{\mathrm{L}}C_{\mathrm{N}}s}{(g_{\mathrm{m6}} + G_{\mathrm{A}} + g_{\mathrm{m5}}g_{\mathrm{m6}}R_{\mathrm{L}} - g_{\mathrm{m6}}G_{\mathrm{A}}R_{\mathrm{L}}) + (2C_{\mathrm{N}} - 2g_{\mathrm{m6}}R_{\mathrm{L}}C_{\mathrm{N}} + g_{\mathrm{m6}}R_{\mathrm{L}}C_{\mathrm{L}} + G_{\mathrm{A}}R_{\mathrm{L}}C_{\mathrm{L}})s - 2R_{\mathrm{L}}C_{\mathrm{N}}C_{\mathrm{L}}s^2}. \tag{22}$$

$$S_{3'2'} = \frac{-2g_m R_L R_C^2}{g_m R_L(R_C^3 + 3R_C^2 + 4R_C + 2) + R_C^3 + 2R_C^2 + R_C}, \quad (32)$$

$$S_{13'} = S_{2'3'} = 0, \quad (33)$$

where R_C is defined by

$$R_C = \frac{R_L}{1 + g_m R_L}. \quad (34)$$

The imbalance between $Z_{12'}$ and $Z_{13'}$ causes imbalances between $S_{2'2'}$ and $S_{3'3'}$, between $S_{23'}$ and $S_{32'}$, and between $S_{12'}$ and $S_{13'}$. This can be resolved by inserting an output buffer as shown in Fig. 6(b). The S-parameters using an ideal output buffer with unity voltage gain and $Z_{12'} \approx 0$ are given by

$$S_{11} = \frac{R_C - 2g_m R_L}{R_C + 2g_m R_L} \quad (35)$$

$$S_{22} = S_{33} = \frac{R_{L2} - 1}{R_{L2} + 1} \quad (36)$$

$$-S_{21} = S_{31} = \frac{4g_m R_L R_C}{2g_m R_L(R_{L2} + 1) + R_C(R_{L2} + 1)} \quad (37)$$

$$S_{12} = S_{13} = S_{23} = S_{32} = 0 \quad (38)$$

Therefore, the buffer ensures perfectly balanced operation and port isolation. Of course, the buffer drives an external 50-Ω load, improving conversion gain and maximum output power. When the designer knows that the next stage is a buffer or an active differential circuit that satisfies $Z_{12} \approx 0$, the choice of the current-mirror input is attractive. In contrast, when the next stage has poor isolation, other input circuit topologies are a more reasonable choice. Examples of other input circuit topologies include Wilson current mirrors, source-coupled pairs, folded cascode amplifiers, and two-stage common source amplifiers. These circuits provide balanced output impedance and in-out isolation. However, other existing alternatives also have drawbacks in other aspects. Wilson current mirrors and source-coupled pairs require higher supply voltages. p-MOSFETs constituting folded cascode amplifiers results in lower bandwidth due to lower f_T. Two-stage common source amplifiers require coupling capacitors and fixed biasing. Finding a new topology that eliminates the buffers while retaining the advantages of low-voltage operation, tightly matched self-biasing, true DC-coupling, and input impedance matching without additional elements is a future challenge.

III. Simulation

A. Verification of Feedback's Effectiveness

The effect of the feedback was confirmed by simulation with Keysight Advanced Design System. First, we performed an S-parameter analysis. The simulation frequency was from 100 MHz to 10 GHz. The value of C_N varied in 9 fF increments from 0 fF to 27 fF. The CMRR was calculated by [43]

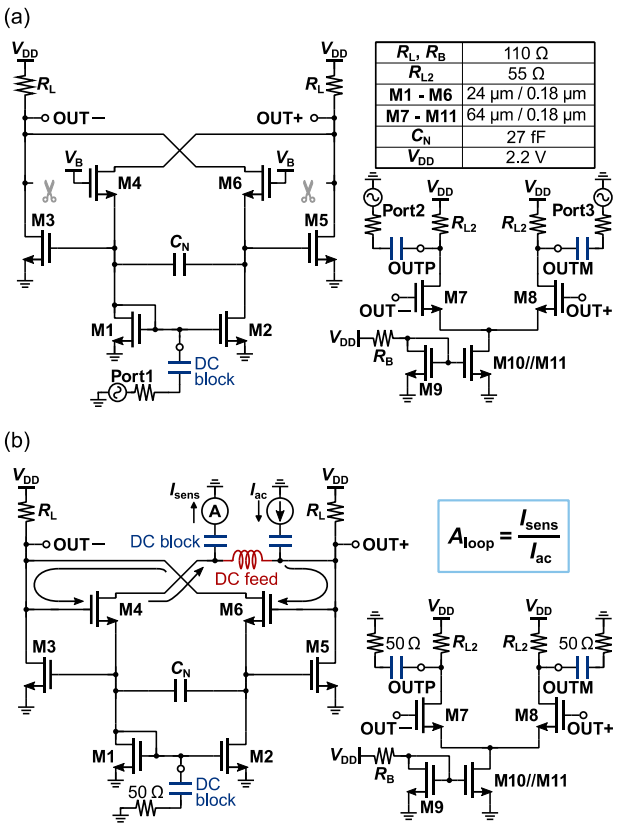


Fig. 7. Simulation test bench. (a) Loop cut to disable the active peaking. (b) AC analysis to determine the loop gain.

$$CMRR = \left|\frac{S_{21} - S_{31}}{S_{21} + S_{31}}\right| = \left|\frac{S_{DS}}{S_{CS}}\right|. \quad (39)$$

where S_{DS} and S_{CS} are the mixed-mode single-ended to differential gain and single-ended to common-mode gain. The loop cut circuit as shown in Fig. 7(a) was also analyzed to investigate the enhancement ratio of the gain-bandwidth product with and without the active peaking. The gate of the M4 and M6 were cut here because the active peaking uses both positive and negative feedback. Ideal voltage sources were connected to the gates of M4 and M6 so that the bias voltage was equal to the closed loop condition. Next, we determined the loop gain by AC analysis. Fig. 7(b) shows a simulation test bench for the AC analysis. The input and output ports were terminated with 50-Ω resistors. The positive feedback loop was cut for small signals at the drain of M4. The current I_{ac} was injected using an AC current source, and the feedback current I_{sens} was detected. The loop gain was determined by

$$A_{loop} = \frac{I_{sens}}{I_{ac}}. \quad (40)$$

Note that if the loop is cut at the drain of M6, the feed-forward path through the current mirror of Balun-A is included, so the exact loop gain cannot be obtained. Alternatively, if the loop is cut at the gate of M4 or M6, the negative feedback loop is also cut, resulting in a change in the loop gain. Therefore, the drain of M4 is most appropriate to determine the loop gain. Fig. 8(a) shows the simulated conversion gain. The dotted line represents

TABLE I
COMPARISON OF PEAKING METHODS

	No. of Zero/Pole	No. of inductor	No. of additional tr.	k_c limitation	BWER†	GBWER††
MPCCT embedded peaking (proposed)	1/2	0	0	No	2.00‡	1.39
Basic RC	0/1	0	0	No	1.00	
Series peaking	0/3	1	0	Yes	1.41–2.52 (k_c = 0–0.3) [38]	
Shunt peaking	1/2	1	0	No	1.83 [39]	
Bridged-shunt GAI peaking	3/4	1	1	No	2.56 [42]	
Bridged-shunt series peaking	2/5	2	0	Yes	3.92 (k_c = 0.4) [38]	
Asymmetric T-coil paeking	1/4	3‡‡	0	Yes	3.93–4.63 (k_c = 0.3–0.1) [38]	

†Bandwidth enhancement ratio with 0-dB gain ripple. ††Gain-bandwidth product enhancement ratio with 0-dB gain ripple. ‡Depending on the DC gain reduction. ‡‡Coupled inductors are available.

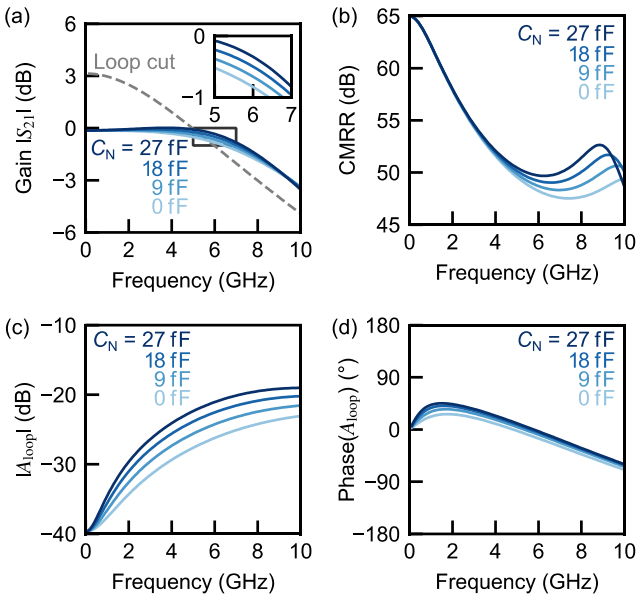


Fig. 8. Simulation results. (a) Conversion gain with and without active peaking. (b) CMRR. (c) Magnitude of the loop gain. (d) Phase of the loop gain.

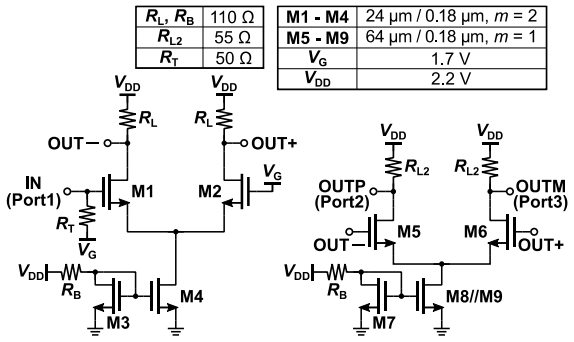


Fig. 9. Schematic of the conventional balun for comparison.

the open-loop condition, and the solid lines represent the closed-loop condition. The low-frequency gain is decreased, and the high-frequency gain is increased due to the active peaking. Large C_N slightly improves the high-frequency gain. The bandwidth was 4.8 GHz and 9.6 GHz in the open and closed loop conditions, and thus, the bandwidth was doubled by the

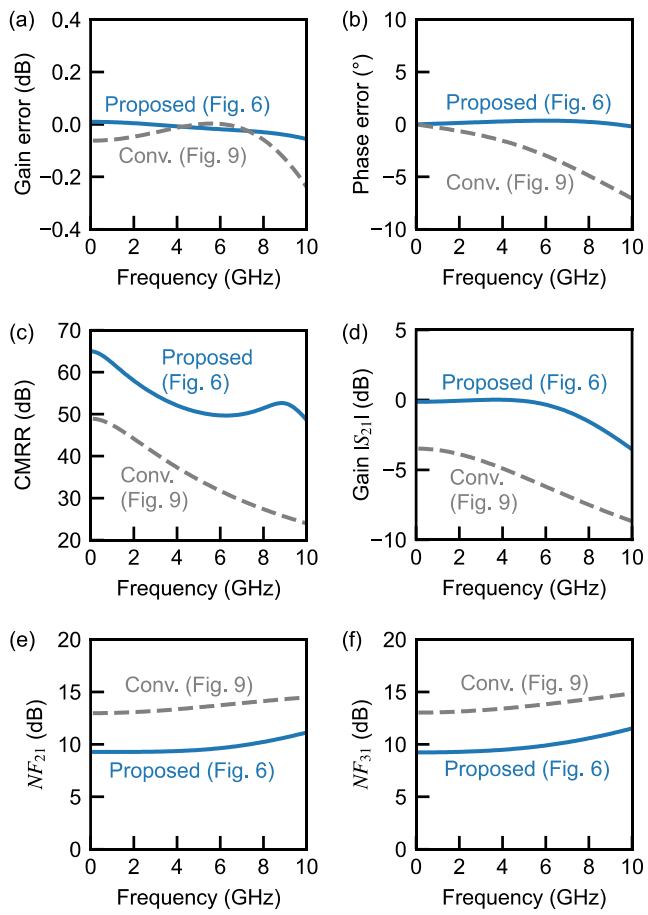


Fig. 10. Simulated comparison results. (a) Gain error. (b) Phase error. (c) CMRR. (d) Conversion gain. (e) Noise figure at port 2. (f) Noise figure at port 3.

active peaking. The conversion gain decreased from 3.1 dB to −0.13 dB due to the negative feedback, but the gain-bandwidth product was enhanced by 39%. Table I shows a comparison with the inductive peaking methods. The values for the bandwidth enhancement ratio are based on the values reported in [38]–[39], [42]. k_c represents the ratio of the drain output capacitance to the total load capacitance [38]. The series peaking, bridged-shunt series peaking, and asymmetric T-coil peaking have excellent bandwidth extension ratios, but they are limited in the range of k_c that can achieve a flat frequency response. The

bridged shunt GAI peaking extends bandwidth by a factor of 2.56 with a single inductor. However, it requires additional transistors and power consumption. The advantage of the proposed MPCCT embedded peaking is that it enhances the bandwidth without adding any inductors and transistors. Fig. 8(b) shows the simulated CMRR. The CMRR at 9 GHz for C_N = 0 fF and 27 fF were 48.5 dB and 52.6 dB. This result suggests that the inserted capacitor improves the CMRR at high frequencies. Fig. 8(c) and (d) show the magnitude and phase of the simulated loop gain. The phase rotation across the bandwidth is less than ±50°, within the range where it can be regarded as positive feedback. The gain margin for C_N = 0 fF and 27 fF were 23.1 dB and 19.0 dB, respectively. Large C_N worsens the gain margin as discussed earlier. This design ensures a gain margin of 10 dB or more, which is necessary for stable operation.

B. Comparison With a Conventional Balun

To evaluate the superiority of the proposed techniques, a simple source-coupled pair shown in Fig. 1(b) was simulated and compared as a widely used topology. The full schematic of the balun for comparison is shown in Fig. 9. To ensure fairness, the input-source coupling pair is composed of n-MOSFETs with a gate width of 24 µm and m = 2, and the load resistance is 110 Ω. The power consumption of the input balun and the common-mode voltage of the output buffer are biased to be the same in Fig. 6 and Fig. 9. The simulated imbalances, conversion gain, and noise figures are shown in Fig. 10. As expected, the proposed balun exhibited better gain and phase errors than the conventional balun. While the CMRR of conventional balun monotonically decreases as the frequency increases, the proposed balun maintains a high CMRR at high frequencies due to the peak formed by C_N. Higher CMRR is obtained even at low frequencies because MPCCT incorporates a phase correction technique using cross-connections. Fig. 10(d) shows that the proposed balun achieves about 3-dB higher DC gain and wider bandwidth than the conventional balun under the same power consumption. Fig. 10(e) and (f) show the simulated noise figures. The simulation results suggest that the noise figure can be improved by about 4 dB. Theoretical analysis of the noise of the proposed balun is a subject for future investigation. Therefore, the simulations demonstrated the superiority of the proposed balun in most aspects. In the next section, we verify whether such performance can be obtained on silicon by experiments.

IV. Experiment

A. Layout Design and Fabrication

The prototype was fabricated in Rohm's 1-poly 5-metal 0.18-µm CMOS process. We slightly tuned the parameters and change the layout from the design described in [30]. The measured transition frequency f_T and maximum oscillation frequency f_{max} of the n-MOSFET were 45 and 65 GHz, respectively [3]. C_N was implemented using a metal-oxide-metal (MOM) capacitor. Fig. 11(a) shows a three-dimensional layout view of the MOM capacitor. The capacitor is composed of metal-2 to metal-4, and the metal-1 plane shields the capacitor

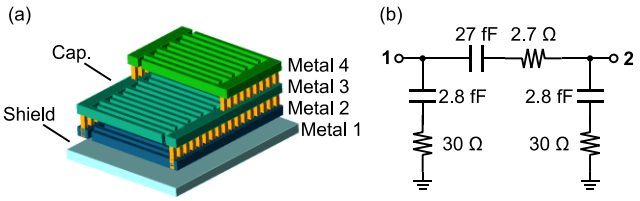


Fig. 11. MOM capacitor. (a) Three-dimensional layout view. (b) Extracted circuit model.

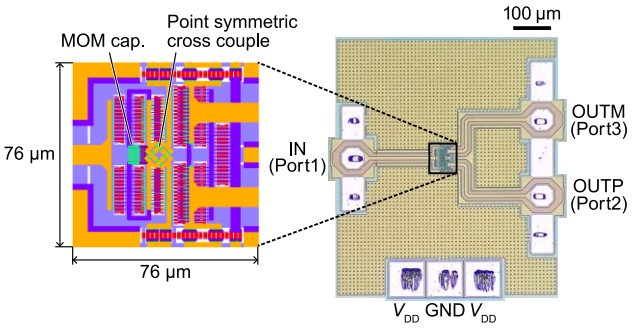


Fig. 12. Layout and chip micrograph of the fabricated balun.

from substrate losses. The capacitor was extracted with Cadence EMX planar solver. Fig. 11(b) shows the extracted circuit model. The MOM capacitor has a small series resistance of 2.7 Ω and a small shunt capacitance of 2.8 fF. The load resistance was implemented with poly resistors that have very little parasitic capacitance. Alternatively, a high open-loop gain is achieved by using active loading with transistors. However, the additional parasitic capacitance introduced by the active load is undesirable because the dominant pole resides at the balun's output node. The simple poly resistance is therefore a better choice. Fig. 12 shows the layout and chip micrograph of the balun. The symmetric layout was realized to reduce gain and phase errors by using a point-symmetric cross couple [44]. The chip area including pads is 0.62 mm × 0.68 mm = 0.42 mm^2, and the core area is only 0.076 mm × 0. 076 mm = 0.0058 mm^2.

B. S-parameters

The three-port *S*-parameters were measured with a four-port vector network analyzer Keysight N5222B. Port 1 was connected to the input, and ports 2 and 3 were connected to the plus output (OUTP) and minus output (OUTM), respectively. The DC power was supplied from Agilent N6705B. Most previous studies evaluated the error by measuring one chip to several chips. However, the systematic error and random error have different causes and should be evaluated separately. In this study, 20 prototype chips were measured, and statistical evaluation was performed for 19 chips, excluding one chip that did not work. All test chips were fabricated on the same shuttle, and lot-to-lot variation was not included. The measured S-parameters for each chip were averaged 16 times with the network analyzer. The calibration error was small enough for the process variation. The statistical evaluation of the gain and phase errors is described in detail in the next subsection. In this subsection, we first present the measurement results of the S-parameters.

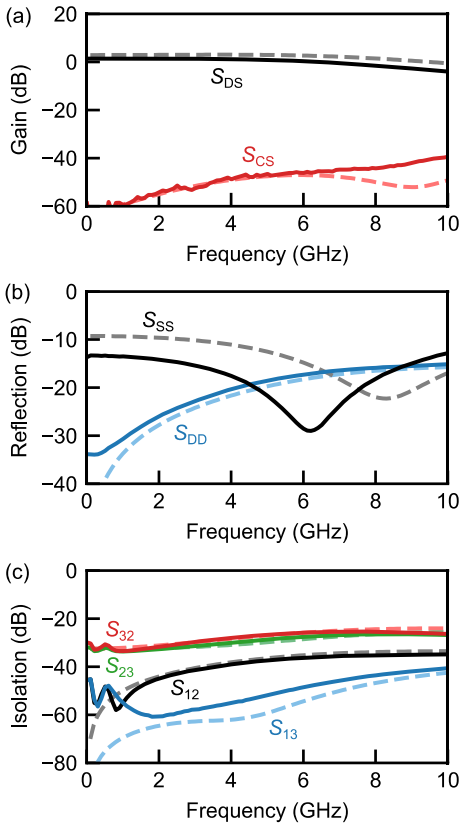


Fig. 13. Measured S-parameters (solid lines: measurement, dashed lines: simulation). (a) Mixed-mode conversion gain. (b) Mixed-mode reflection. (b) Port isolation.

Fig. 13 shows the measured conversion gain, reflection coefficients, and port isolation. All of these are averages of 19 chips. The measured single-ended to differential gain $|S_{DS}|$ was 1.4 dB at 10 MHz. The single-ended voltage gain of each stage extracted by the simulation is 6.8 dB for the balun, −3.3 dB for the buffer, and −3.6 dB for excess attenuation due to impedance mismatch at 10 MHz. The measured and simulated 3-dB bandwidth was 8.0 GHz and 9.6 GHz, respectively. The slight gain and bandwidth reduction from the simulation are due to the layout-dependent parasitics. Both input and output reflection coefficients were less than −10 dB. The error between the simulated and measured S_{SS} is due to model errors of the 24-μm width transistors, which has been verified by the measurement of the test elements. The current mirror input stage ensures broadband matching without an additional matching network. The input impedance at 100 MHz is 33+j0.058 Ω that is smaller than 50 Ω due to negative feedback. At higher frequencies, the input impedance increases as the negative feedback become weaker: the input impedance at 6 GHz is 47+j1.3 Ω. At even higher frequencies, reflections increase due to the capacitive reactance component: the input impedance at 8 GHz is 46−j12 Ω. The capacitive reactance is mainly composed of the transistor's parasitics and C_N itself. The input reflection is lower than −10 dB up to 10 GHz, and we can see that the input node is not dominant to determine the bandwidth. The port isolation was better than −25 dB. The imbalance between S_{12} and S_{13} is due to the current mirror input stage. This imbalance is hardly a problem since the magnitude of S_{12} and S_{13} is smaller than −35 dB thanks to the output buffer.

C. Statistical Evaluation of the Errors

The random component due to manufacturing variation can be a dominant factor in determining the gain and phase errors. The purpose of this subsection is to separately evaluate the systematic and random components of the error from a set of measurement results of fabricated chips. The 3σ rule is usually used to evaluate the manufacturing variability of integrated circuits. When the distribution of the measured metrics is Gaussian, 99.7% of the data falls within the μ±3σ range. μ and σ represent the mean and standard deviation of the measurement dataset. In the gain and phase errors, we can find the systematic and random components by calculating the average and 3σ of the dataset. On the other hand, the CMRR is a better metric of balun performance because it can evaluate gain and phase at once. However, the distribution of the CMRR is generally not a Gaussian distribution. This is intuitive since CMRR corresponds to the inverse of the magnitude of the error vector between differential outputs, and it is ideally infinite. Yu *et al.* [45] assume that the amplitude error between the differential outputs follows a Gaussian distribution. In that case, the distribution of CMRR is represented by [45, eq. (37)]. From this distribution of the CMRR, the 99.7% limit of the CMRR can be calculated [45, eqs. (54), (57)]. However, the analysis in [45] assumes the common-mode gain and differential gain are scalar quantities, which do not include the phase. When the phase is included, the error between the differential outputs becomes a vector in the complex plane. This paper extends the analysis of the random CMRR to the complex plane to reveal the 99.7% limit when the error is a vector. First, we have a set of measured differential gain $\{S_{DS,1}, S_{DS,2}, ..., S_{DS,N}\}$ and a set of common-mode gain $\{S_{CS,1}, S_{CS,2}, ..., S_{CS,N}\}$. N represents the sample size. The systematic differential gain S_{DS}^{d} is estimated as the mean vector of the differential gain as follows:

$$S_{DS}^{d} = \frac{1}{N}\sum_{n=1}^{N} S_{DS,n}\,. \tag{41}$$

In [45, eqs. (15), (16), (23)–(25)], a variable y is defined as a common-mode gain normalized by the systematic differential gain. y means a normalized amplitude error for the one-dimension case, and its distribution is Gaussian. For the S-parameters, y is a vector in the complex plane, and for the n-th device it is obtained by

$$y_n = \begin{bmatrix} \mathrm{Real}\left(S_{CS,n}/S_{DS}^{d}\right) \\ \mathrm{Imag}\left(S_{CS,n}/S_{DS}^{d}\right) \end{bmatrix}. \tag{42}$$

This normalization is based on the assumption that the random component of the differential gain is sufficiently small compared to the magnitude of the differential gain. y_n means the normalized error vector between the differential outputs. The CMRR is given by

$$CMRR = \frac{1}{|y|}. \tag{43}$$

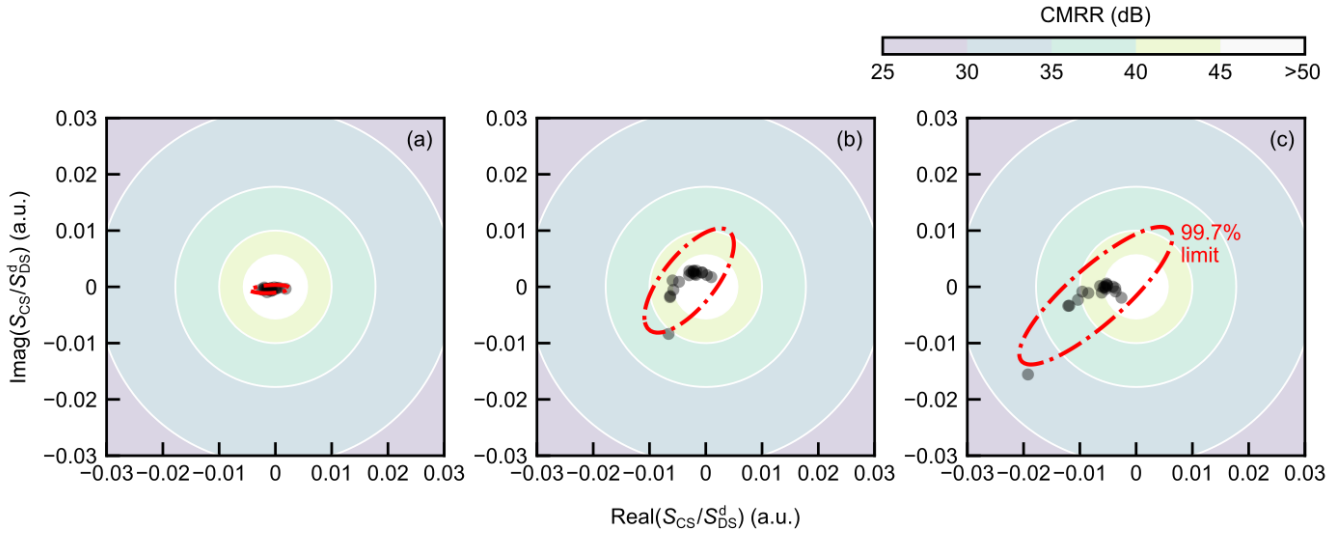


Fig. 14. Measured normalized error vector y_n for 19 chips (dots) and 99.7% equiprobability ellipses (red chain lines). (a) 10 MHz. (b) 4 GHz. (c) 8 GHz.

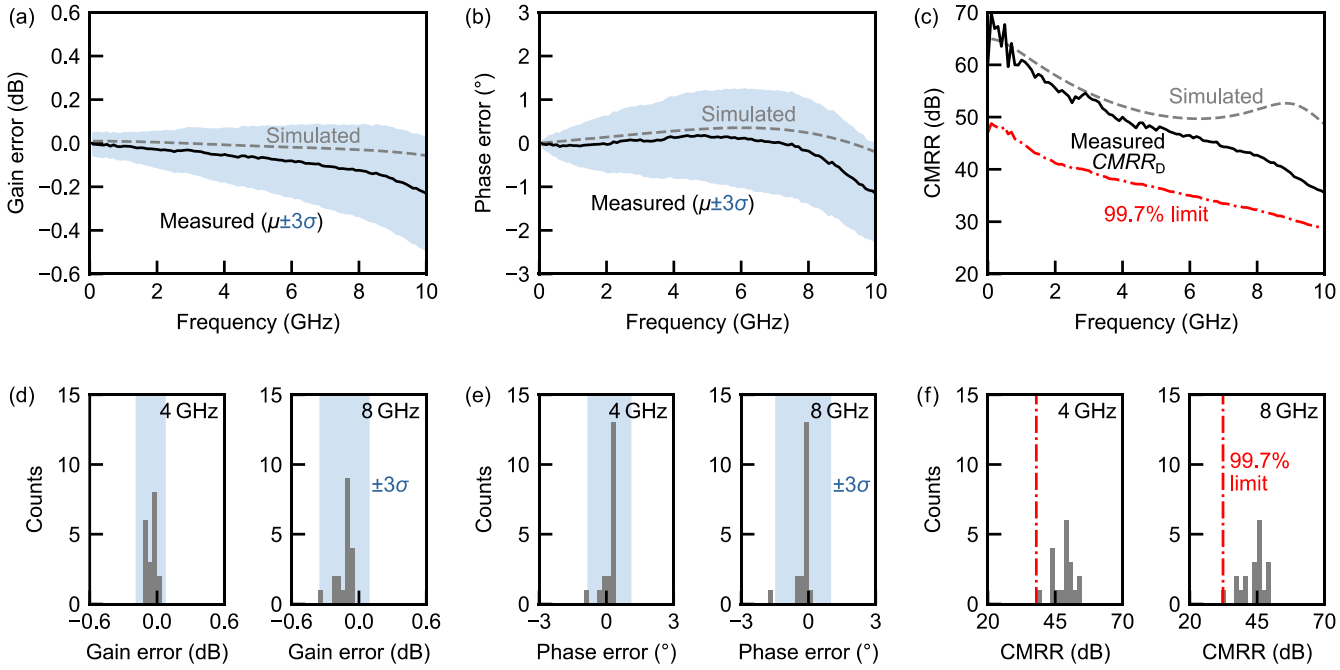


Fig. 15. Imbalance measurement results for 19 chips. (a) $\mu\pm3\sigma$ of the gain error. (b) $\mu\pm3\sigma$ of the phase error. (c) Systematic CMRR and 99.7% limit of the CMRR. (d) Histogram of the gain error at 4 GHz and 8 GHz. (e) Histogram of the phase error at 4 GHz and 8 GHz. (f) Histogram of the CMRR at 4 GHz and 8 GHz.

y_n are scattered in the complex plane and we assume that their distribution is two-dimensional Gaussian as the natural extension of [45, eq. (30)]. The probability density function of y is given by

$$P(y) = \frac{1}{2\pi\sqrt{\det(\Sigma)}} \exp\left[-\frac{1}{2}(y-d)^{\mathrm{T}}\Sigma^{-1}(y-d)\right], \quad (44)$$

where Σ is a variance-covariance matrix for the real and imaginary parts of y_n, and d represents the systematic normalized error vector can be estimated as a mean vector of y_n as follows:

$$d = \frac{1}{\mathrm{N}}\sum_{n=1}^{\mathrm{N}} y_n . \quad (45)$$

The systematic CMRR is given by

$$CMRR_{\mathrm{D}} = \frac{1}{|d|}. \quad (46)$$

In the one-dimension case as described in [45, eqs. (54), (57)], the 99.7% range can be calculated from the 3σ range of the normalized error. For the two-dimensional Gaussian, the 99.7%

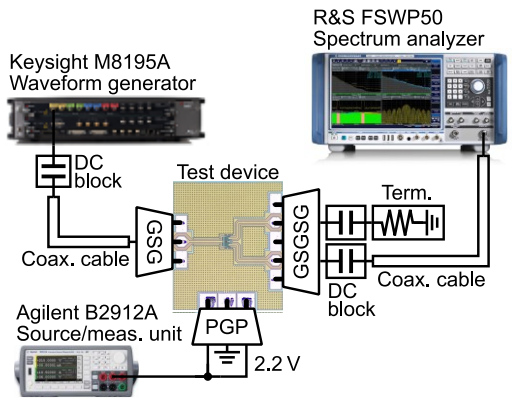


Fig. 16. Setup for the large signal measurements.

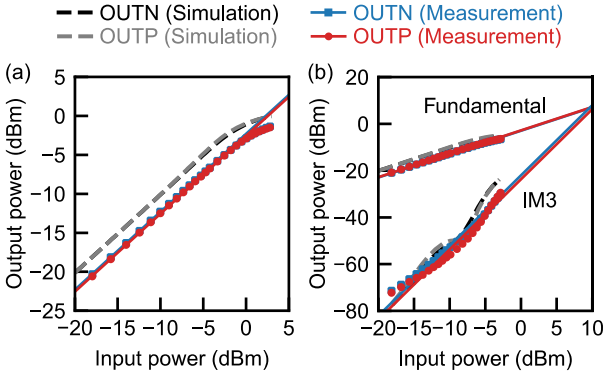


Fig. 17. Large signal measurement results. (a) Single-tone. (b) Two-tone.

limit is given by an equiprobability ellipse with a constant probability density value. The equiprobability ellipse is the locus of points for which the Mahalanobis' distance D from the mean vector is constant. D is given by

$$D = \sqrt{(y-d)^{\mathrm{T}}\Sigma^{-1}(y-d)}. \qquad (47)$$

When the dataset is a two-dimensional Gaussian, the distribution of D^2 is a chi-square distribution with two degrees of freedom. Thus, the 99.7% equiprobability ellipses can be calculated by $D = 3.409$. The CMRR is obtained as the reciprocal of the Euclidean distance from the origin in the complex plane of y. Therefore, the 99.7% limit of the CMRR is determined by the worst point of the CMRR on the 99.7% equiprobability ellipse. Fig. 14 shows measured normalized error vectors and their 99.7% limits. The black dot represents y_{n} and the mean vector d is located at the center of the ellipse. At higher frequencies, the scattering of y_{n} increases and CMRR decreases. The 99.7% limits of the CMRR at 10 MHz, 4 GHz, and 8 GHz are 47 dB, 38 dB, and 32 dB, respectively. Fig. 15 summarizes the measured error characteristics. Fig. 15(a) and (b) show measured gain and phase errors. The gray dashed lines represent the simulation results, and the black solid lines represent the estimated systematic error. The measured systematic error agrees well with the simulation results. The maximum systematic gain error was −0.12 dB and the maximum systematic phase error was −0.18° across the bandwidth. The blue-filled area represents the $\pm 3\sigma$ range for the 19 chips. The random error increased as the frequency increased, and we can find that the random error dominates at high frequencies. Fig. 15(d) and (e) show histograms of the errors at 4 GHz and 8 GHz. The 99.7% range of the gain error at 8.0 GHz was $\mu+3\sigma = -0.12+0.20$ dB and $\mu-3\sigma = -0.12-0.21$ dB. The phase error at 8 GHz was $\mu\pm3\sigma = -0.18\pm1.17°$. Fig. 15(c) shows measured CMRR. The black solid line represents the systematic error estimated by (45). The systematic CMRR agrees with the simulation results. The deviation from the simulation at high frequencies corresponds to the systematic gain error and phase error increasing at high frequencies. The red chain line represents the 99.7% limit calculated with the equiprobability ellipses. The balun achieved a systematic CMRR of 43 dB and a 99.7% limit of 32 dB.

D. Large Signal Characteristics

The large signal characteristics of the balun were evaluated by single-tone and two-tone measurements. Fig. 16 shows the setup for the large signal measurements. A Keysight M8195A arbitrary waveform generator was connected to the input, and a Rohde & Schwarz FSWP50 spectrum analyzer was connected to one output port. The other output port was 50-Ω terminated via a DC block. Both OUTP and OUTM were measured by switching the connection of the termination and spectrum analyzer. First, a 1-GHz sine wave was inputted, and the output power of the fundamental wave was measured in the single-tone measurement. The input power was swept from −18.0 dBm to 2.8 dBm. The RF cable losses were measured beforehand using a network analyzer and de-embedded after measurement. Fig. 17(a) shows the results of the single-tone measurements. The measured output P1dB was −2.0 dBm at the OUTM and −1.8 dBm at the OUTP. The error between the OUTP and OUTM power was less than 0.27 dB across the sweep range. The measured conversion gain was about 2 dB less than the simulation. This is due to model error of the transistors and process variation. Next, sine waves of 1.0 GHz and 1.1 GHz were inputted for the two-tone measurement. The amplitude of each wave was equal, and the sweep range was from −18.8 dBm to −3.5 dBm. Fig. 17(b) shows the results of the two-tone measurement. The measurement results are in good agreement with the simulation. The measured IIP3 was 9.6 dBm at the OUTM and 10.5 dBm at the OUTP. The characteristics of the OUTP and OUTM were in excellent agreement, confirming that the proposed technique works well under large signal conditions.

E. Performance Comparison

Table II lists the cutting-edge active baluns for performance comparison. The baluns presented in [22], [46], and [47] were fabricated in high-performance BiCMOS technology. They offer superior bandwidth of 50 GHz or over. Huynh *et al.* [47] achieved a low power consumption with a simple circuit topology combining a common collector and common emitter circuit. However, it lacks imbalance correction, resulting in significant gain and phase errors. On the other hand, the baluns in [21], [26], [28], and [48] were fabricated in CMOS technology. Bhat

TABLE II
COMPARISON WITH THE CUTTING-EDGE ACTIVE BALUNS

Reference	This work '23	[46] '20 *BCICTS*	[22] '19 *BCICTS*	[47] '16 *MWCL*	[48] '22 *J.SSC*	[26] '18 *MOTL*	[28] '12 *ASSCC*	[21] '09 *MWCL*
Technology	0.18-µm CMOS	0.13-µm BiCMOS	0.13-µm BiCMOS	0.18-µm BiCMOS	22-nm FDSOI	65-nm CMOS	65-nm CMOS	0.13-µm CMOS
f_T/f_{max} (GHz)	45/65	250/340	300/450	N.R.	N.R.	N.R.	N.R.	91/108
B.W. (GHz)	DC–8.0	3–60	DC–>70	DC–50††	0.005–5.55	1.0–1.2	53–65	2–40‡‡‡
B.W./f_{max} (GHz)	0.12	0.17	>0.16	N.R.	N.R.	N.R.	N.R.	0.35
Inductive elements	Un-used	Un-used	Used	Used	Un-used	Un-used	Used	Used
Core area (mm^2)	0.0058	0.042	0.03†	0.11†	1.1	0.0091‡	0.26	0.37†
Gain (dB)	1.4**	2.3*	3.6**	−1.1* (port 3)	11**	4*	6.1*	1*
Gain error (dB)	$\mu+3\sigma=-0.12+0.20$ $\mu-3\sigma=-0.12-0.21$	0.65	0.2	1	0.5	1.4	0.36	0.5
Phase error (°)	$\mu\pm3\sigma=-0.18\pm1.17$	3.2	5	10	5	3.5	2.2	10
CMRR (dB)	$CMRR_D=43$ (99.7% limit) = 32	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.
IIP3 (dBm)	10	N.R.	N.R.	7 (port 3)	14	N.R.	N.R.	N.R.
OP1dB (dBm)	−2*	−5.2*	0.8**	−1.6* (port 3)	N.R.	N.R.	N.R.	N.R.
DC power (mW)	88‡‡	37	144	14.4	925	2.6	11.6	40

†Estimated from the micrograph. ††The gain variation is greater than 5 dB. ‡Excluding the input and output matching network. ‡‡19 mW for the input balun, 45 mW for the buffer, and 24 mW for the bias circuit. ‡‡‡No input impedance matching. *Single-ended. **Differential.

et al. [48] integrated output drivers that provided high conversion gain and output power at the expense of the power consumption and chip area. Choi *et al*. [26] and Chou *et al*. [28] report low power consumption, but the operating bandwidth is limited. Huang *et al*. [21] report a wide bandwidth of 2-40 GHz despite using 0.13-µm CMOS technology due to the inductive elements that consume a large chip area. The balun reported in this paper has a small chip area of 0.0058 mm^2. The bandwidth of the active balun in this study is 8.0 GHz, but this can be improved by using faster devices or integrating inductive elements. Since the f_{max}-normalized bandwidth is 0.12, it expects a bandwidth of 36-GHz using an advanced process with a f_{max} of 300 GHz. Furthermore, A 66-GHz bandwidth can be expected by applying the shunt peaking that extends the bandwidth by a factor of 1.83. Inductive peaking, however, causes phase rotation, which breaks the positive feedback and increases the imbalance. It is hoped that this trade-off will be resolved in future studies. The power consumption of the developed balun consists of 19 mW for the input balun, 45 mW for the output buffer, and 24 mW for the bias circuit, for a total of 88 mW. Except for the bias circuit, 70% of the power is consumed by the buffer. This is because our target application, an analog multiplexer for optical transmitters, requires high output swing and linearity. The developed balun achieves a 1-V_{pp} output swing in differential at the expense of power consumption. In addition, there is a trade-off between output power and bandwidth. In this balun, the input capacity of the buffer determines the bandwidth, as mentioned above. It is possible to design the balun to sacrifice output amplitude to reduce power consumption and increase bandwidth. The gain and phase errors of the developed balun are much smaller than those in previous studies even if including the process variation of $\pm3\sigma$. There are no CMRR reports listed in the table, except for this study. Some have small gain errors but large phase errors, and vice versa. The CMRR is useful because it allows a unified comparison of both gain and phase errors. Also, as reported in subsection IV-C, process variation can be a dominant factor in determining the errors, and therefore, statistical evaluation is also important.

V. CONCLUSION

An active balun using positive and negative feedback for imbalance correction and active peaking was analyzed and evaluated. The positive feedback loop of MPCCT eliminated common-mode signals by making the node impedance for differential signals larger than that for common-mode signals. The high-frequency CMRR was improved by adding a capacitor at the expense of the gain margin. We established that the positive and negative feedback of the MPCCT is available for active peaking. This active peaking doubled the bandwidth and enhanced the gain-bandwidth product by 39% without using any additional inductors and transistors. The active peaking reduced the core area down to 0.0058 mm^2. In addition, a self-bias scheme with a current mirror was presented, which provided good current balance without using DC cut capacitors and extra bias voltages. The good current balance reduced gain and phase errors. The measurements demonstrated a superior gain error of $\mu+3\sigma=-0.12+0.20$ dB and $\mu-3\sigma=-0.12-0.21$ dB, and a phase error of $\mu\pm3\sigma=-0.18\pm1.17°$. We extended the theory of the random CMRR to obtain a 99.7% limit of the CMRR. The balun achieved a 99.7% limit of the CMRR greater than or equal to 32 dB across the bandwidth. Therefore, these techniques contribute to developing high-precision and low-cost active baluns.

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